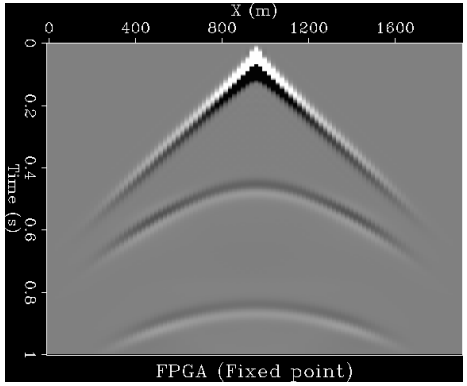
www.maxeler.com

1 Down Place
Hammersmith
London UK

530 Lytton Ave.
Palo Alto
CA USA

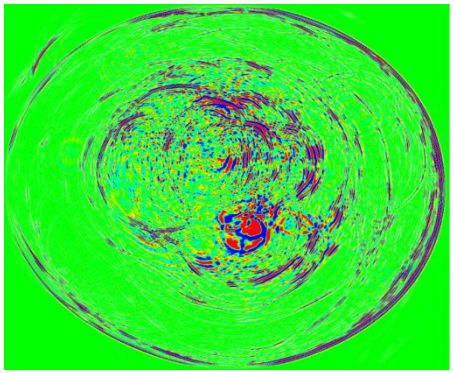
Deployed Maximum Performance Computing

customers comparing 1 box from Maxeler (in a deployed system) with 1 box from Intel



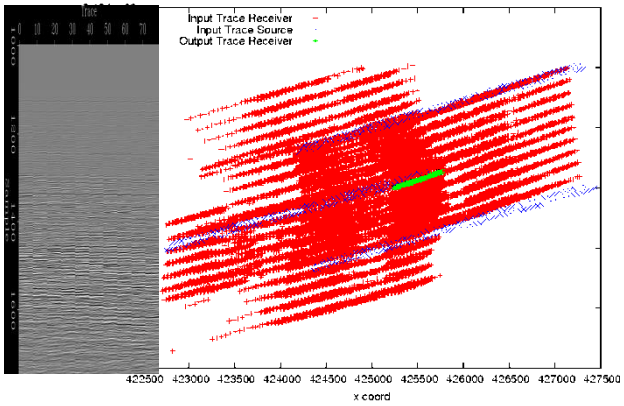
Customer 1

App1 19x and App2 25x



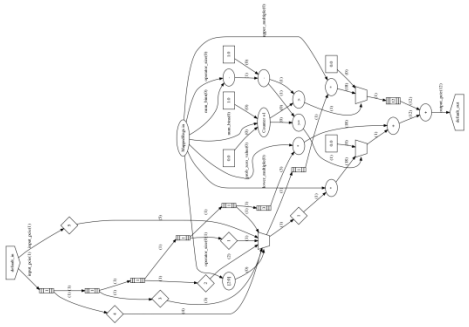
Customer 2

1.2GB/s per card



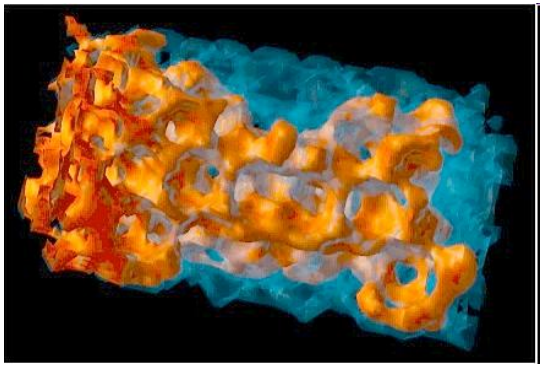
Customer 3

App1 22x, App2 22x



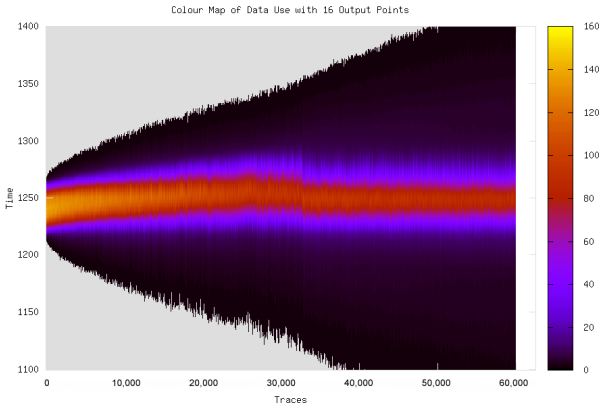
Customer 4

App 32x and App2 29x



Customer 5

30x



Customer 6

App1 26x and App2 30x

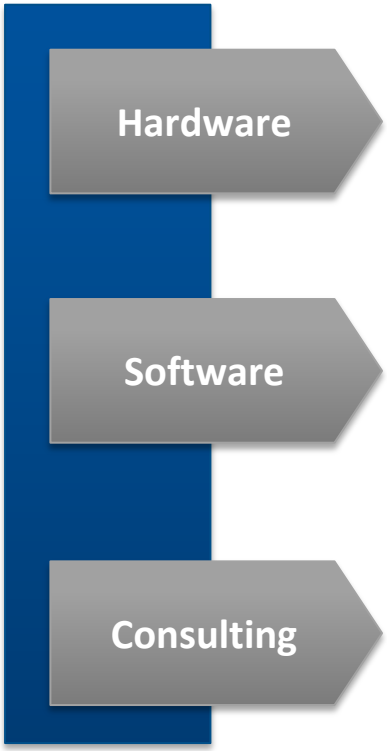
MAXELER Technologies

What Maxeler do

- Maxeler delivers bespoke dataflow HPC solutions

  => An HPC Computing Appliance for “structured Big Data”

- Building the HPC compute fabric based on the application in a multi-disciplinary, data-centric approach



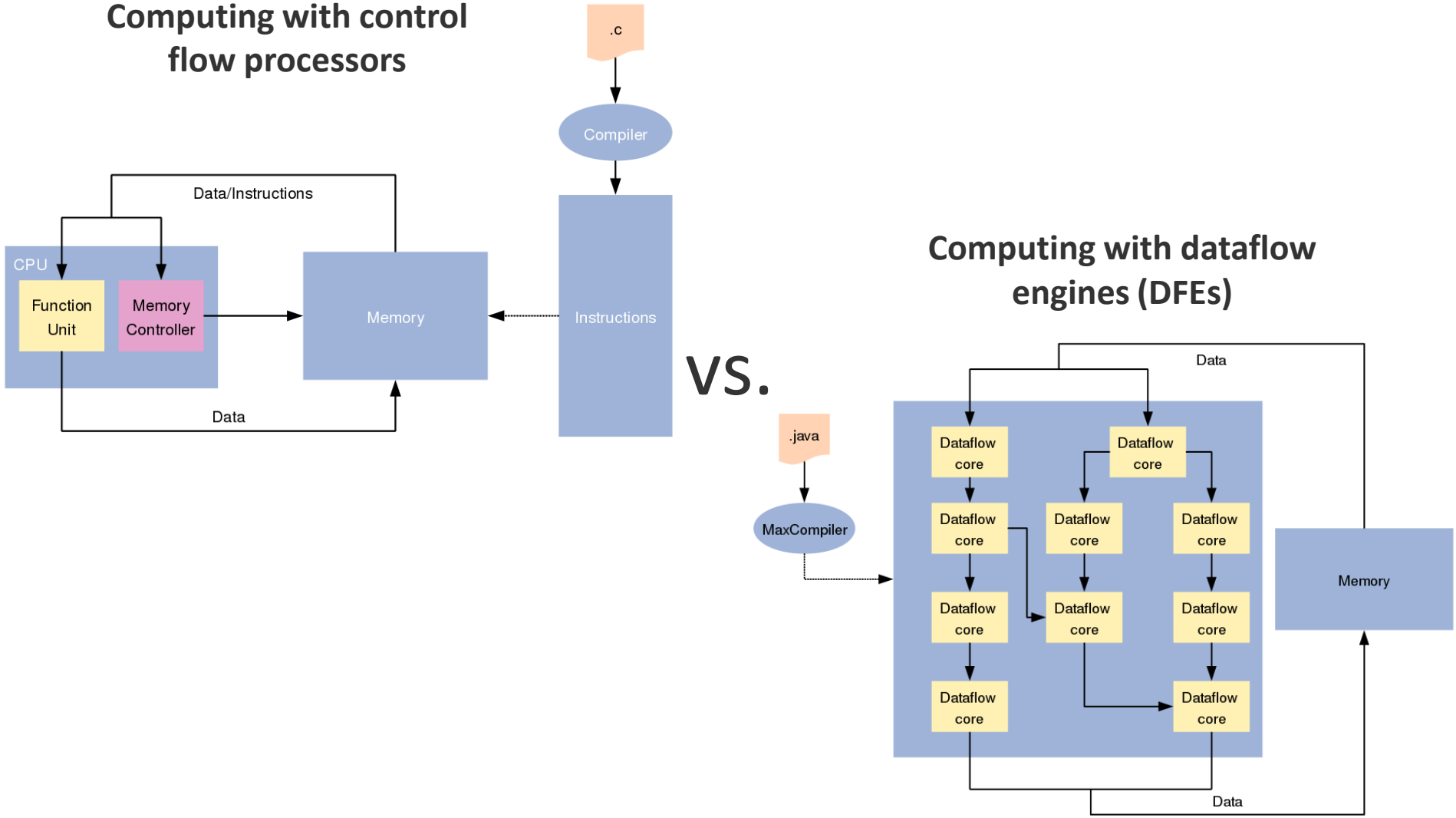
- Building 1U boxes, Workstations and the cards inside.
- Building custom large memory systems to deal with Big Data
- Integrating rack system with networking and storage.

- Integrated environment brings bespoke dataflow computing to high end HPC users
- Dataflow programming in Java and Eclipse IDE

- HPC System Performance Architecture
- Algorithms and Numerical Optimization
- Integration into business and technical processes

Dataflow Computing

What is Dataflow Computing?

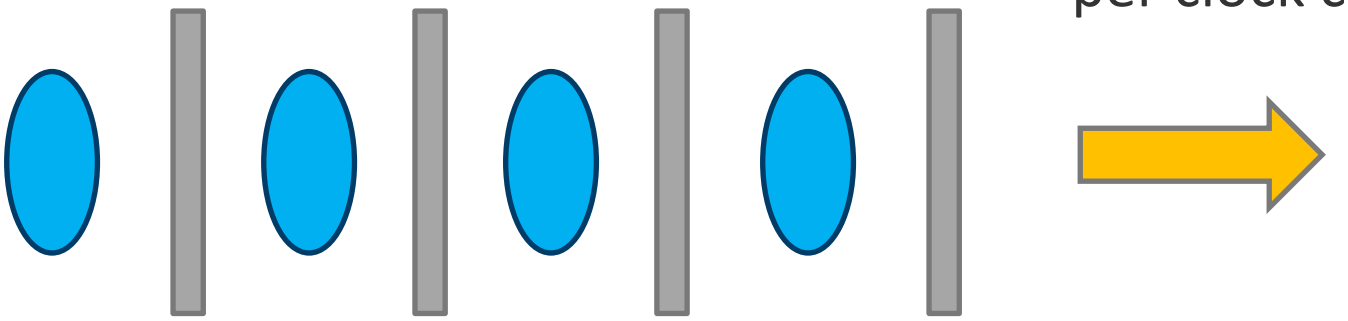


MAXELER Technologies

Technology

MAXELER DATAFLOW COMPUTING

One result
per clock cycle



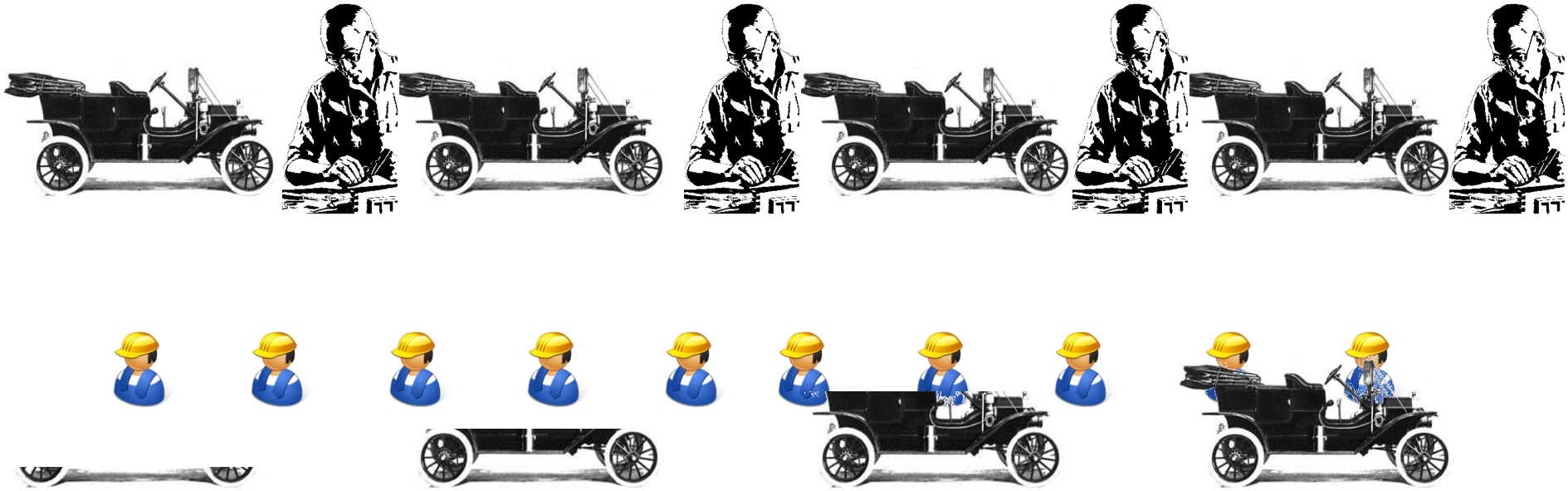
Dynamic (switching) Power Consumption:

$$P_{avg} = C_{load} \cdot V_{DD}^{\ 2} \cdot f$$

Minimal frequency f achieves maximal performance, thus for a given power budget, we get Maximum Performance Computing (MPC)!

Explaining Control Flow versus Data Flow

Analogy 1: The Ford Production Line



- Experts are expensive and slow (control flow)
- Many specialized workers are more efficient (data flow)

Maxeler Hardware Solutions

MPC C Series

CPUs plus DFEs

Intel Xeon CPU cores and up to 6 DFEs with 288GB of RAM

MPC X Series

DFEs shared over Infiniband

Up to 8 DFEs with 384GB of RAM and dynamic allocation of DFEs to CPU servers

MPC N Series

Low latency connectivity

Intel Xeon CPUs and 1-2 DFEs with up to six 10Gbit Ethernet connections

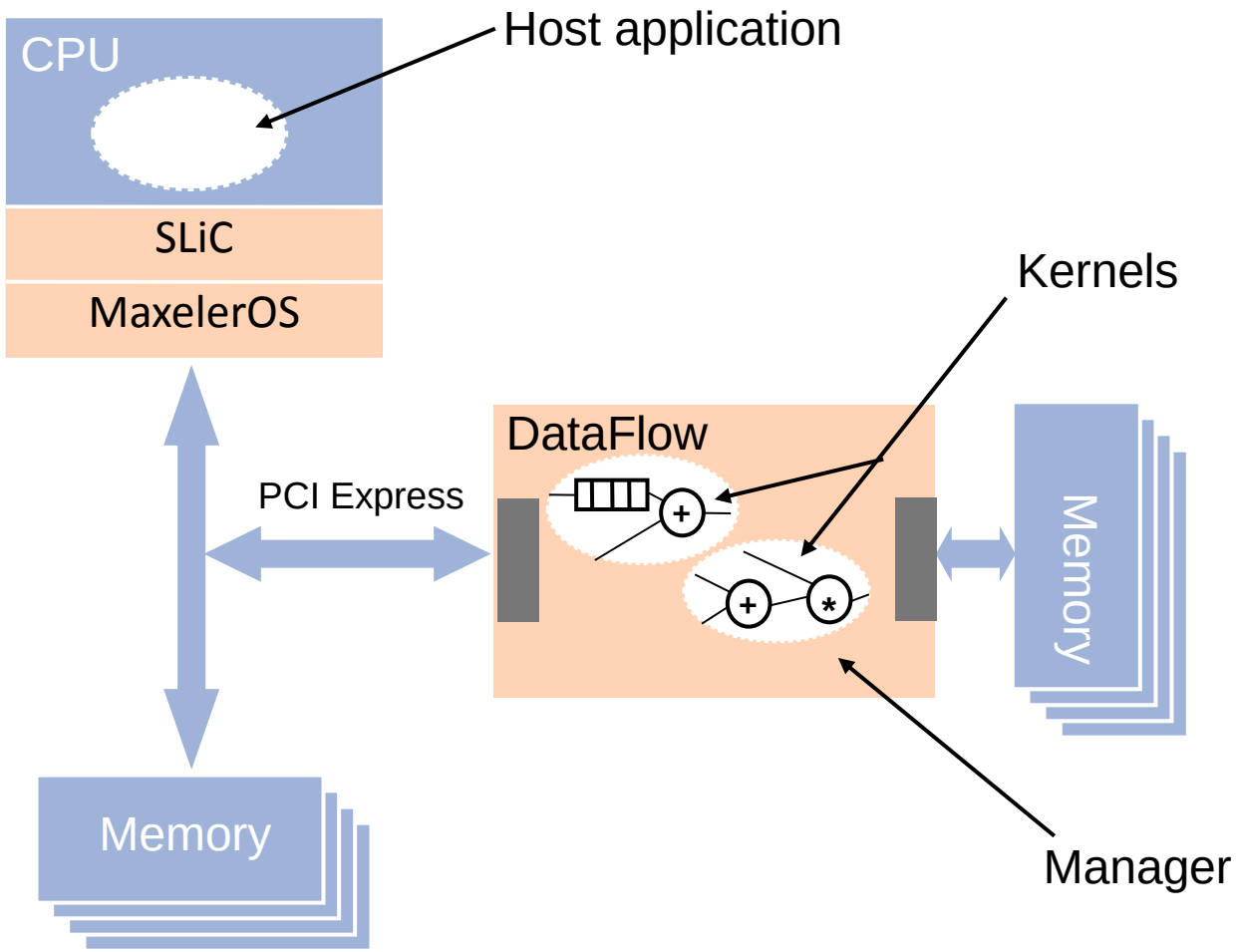
MaxWorkstation

Desktop development system

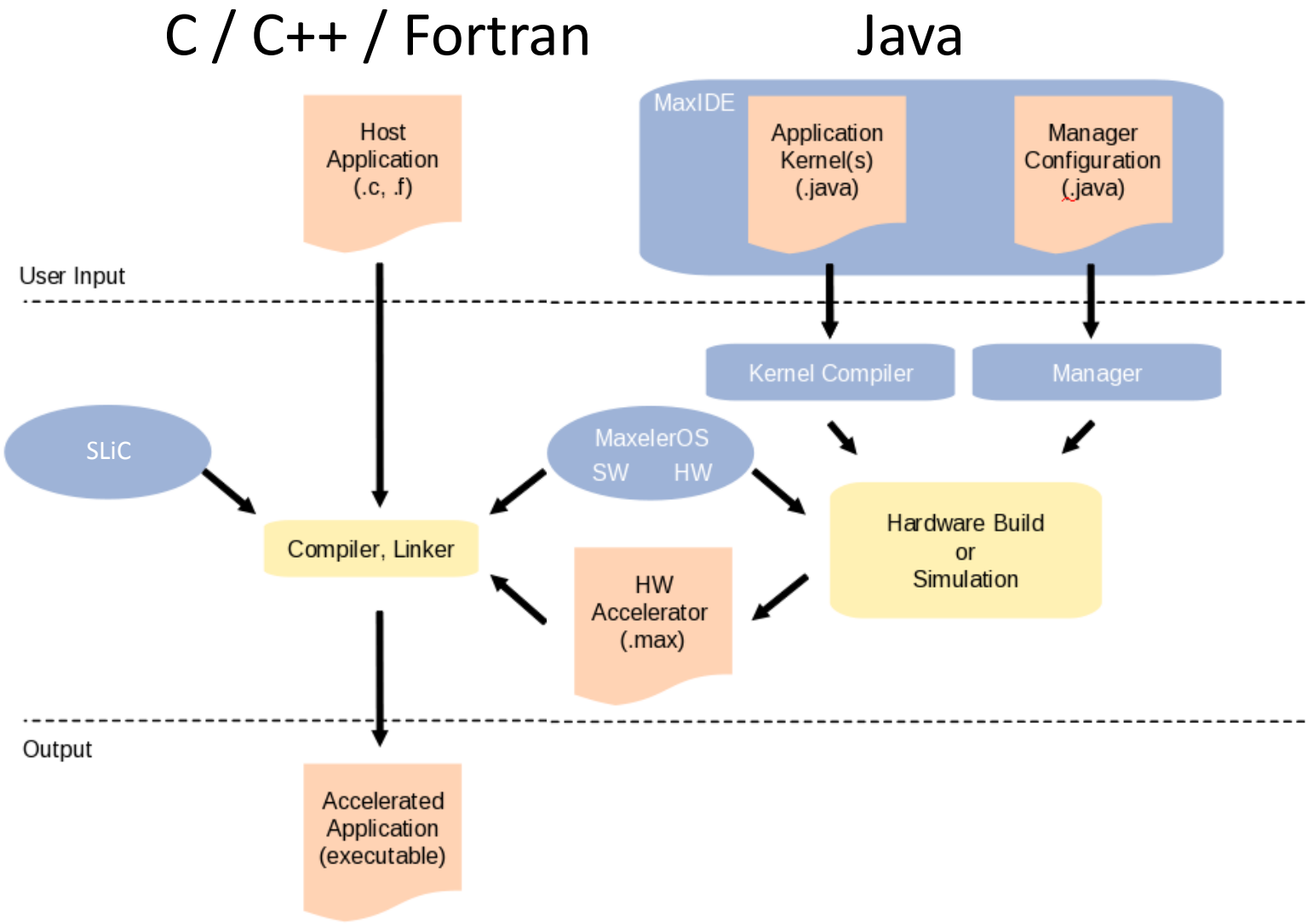
MaxCloud

On-demand scalable accelerated compute resource, hosted in London

Maxeler Application Components



Programming with MaxCompiler



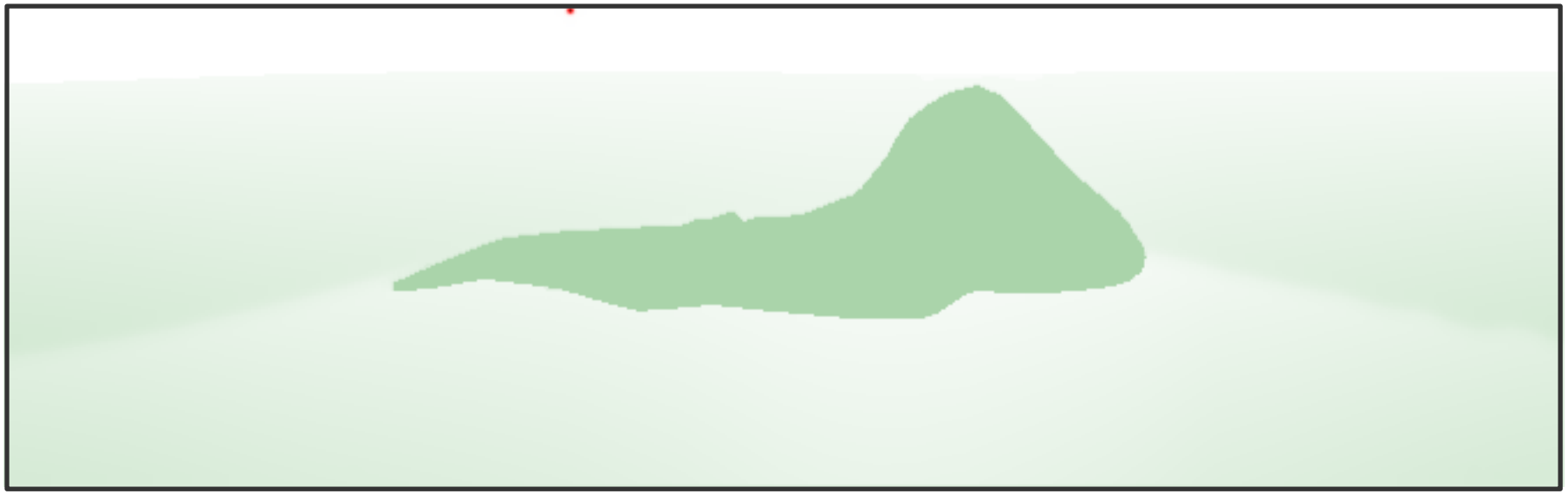
MAXELER Technologies

Cluster-level management

- Deploying Maximum Performance Computing requires considering cluster resource allocation and scheduling
- Maxeler create custom job-management systems to manage clusters
- MaxQ Cluster Management System
  - Job Distribution
  - Designed to manage thousands of CPU cores and terabytes of memory
  - Dynamically reallocates resources during execution
  - Logging of running processes
  - Remotely Attach to running processes

Example Accelerated Applications

Seismic Imaging



- Running on MaxNode servers
  - 8 parallel compute pipelines per chip
  - 150MHz => low power consumption!
  - 30x faster than microprocessors

An Implementation of the Acoustic Wave Equation on FPGAs

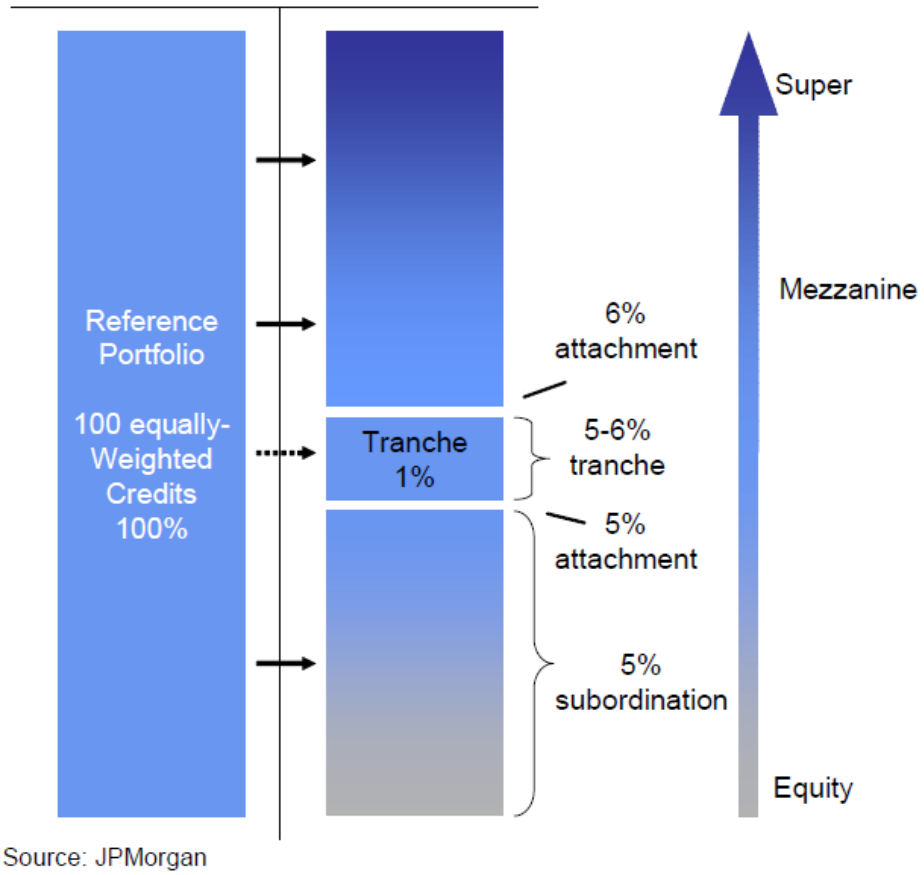
T. Nemeth[†], J. Stefani[†], W. Liu[†], R. Dimond[‡], O. Pell[‡], R.Ergas[§]

[†]Chevron, [‡]Maxeler, [§]Formerly Chevron, SEG 2008

JP Morgan Credit Derivatives Pricing

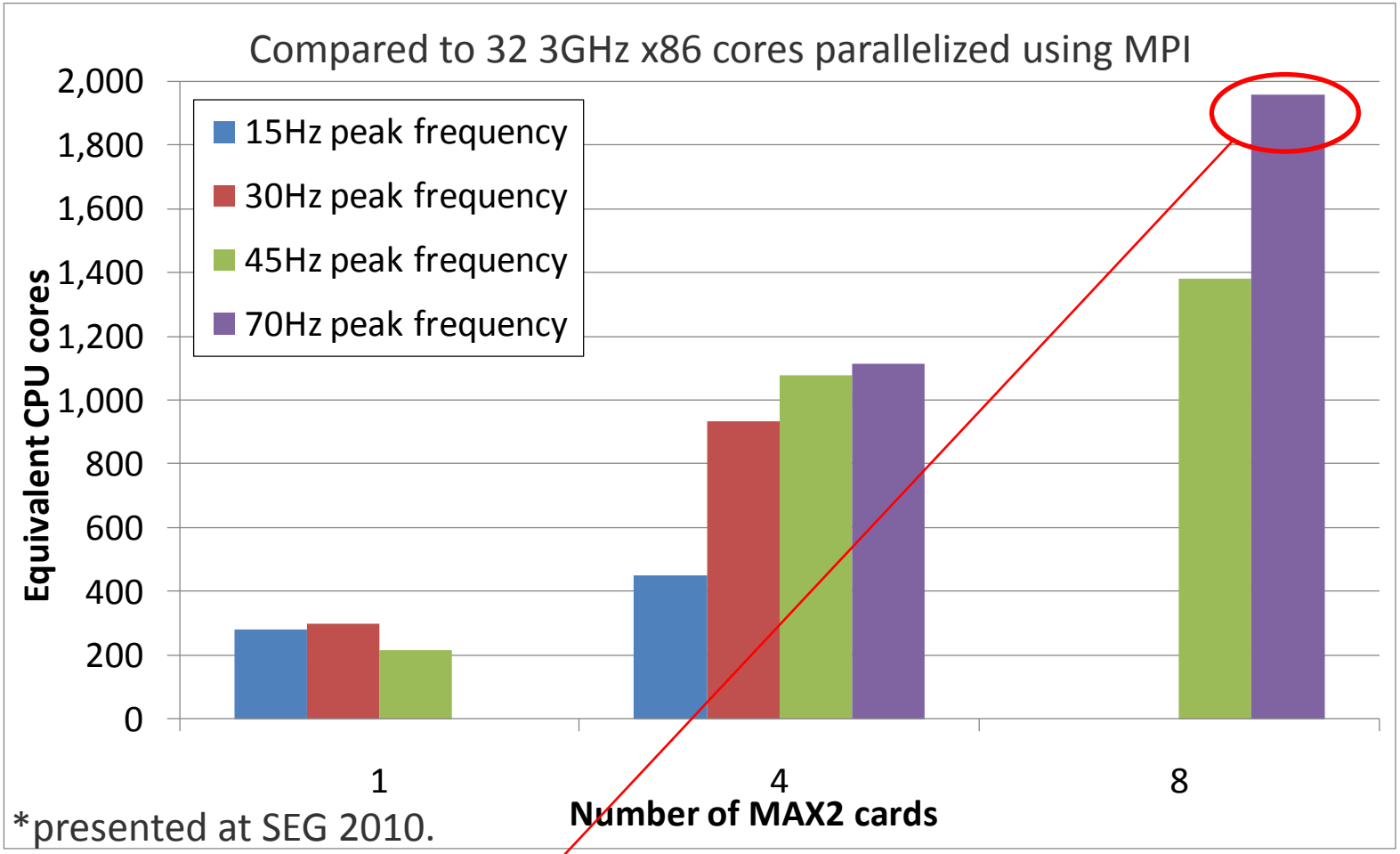
O. Mencer and S. Weston, 2010

- Compute value of complex financial derivatives (CDOs)
- Typically run overnight, but beneficial to compute in real-time
- Many independent jobs
- **Speedup: 220-270x**
- Power consumption per node drops from 250W to 235W/node



Source: JPMorgan

3000³ Modeling



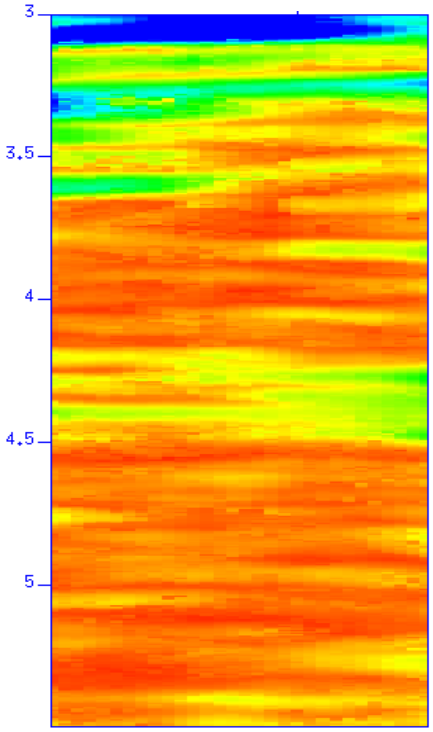
8 Full Intel Racks ~100kWatts => Single 3U Maxeler System <1kWatt

MAXELER Technologies

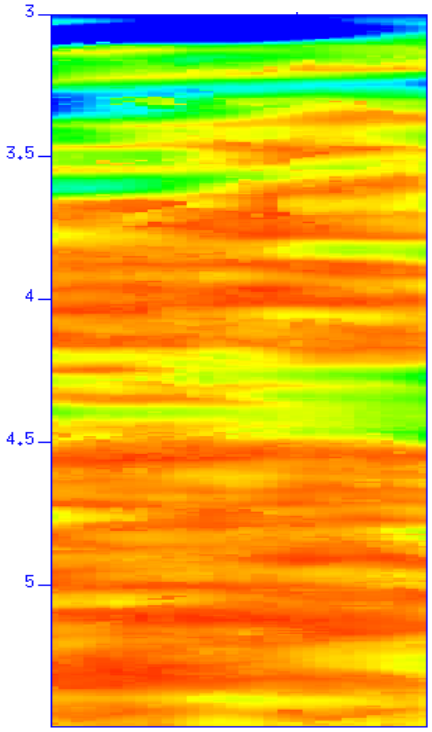
CRS Results

- Performance of one MAX2 card vs. 1 CPU core
  - Land case (8 params), speedup of 230x
  - Marine case (6 params), speedup of 190x

CPU Coherency



MAX2 Coherency

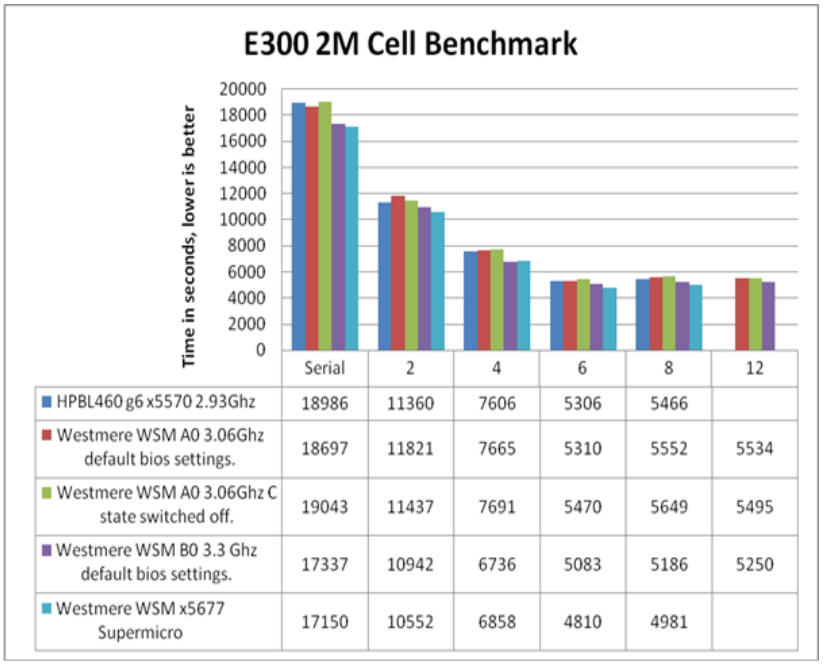


Sparse Matrix Solving with Maxeler

O. Lindtjorn et al, HotChips 2010

Given matrix **A**, vector *b*, find vector *x* in **A***x* = *b*.

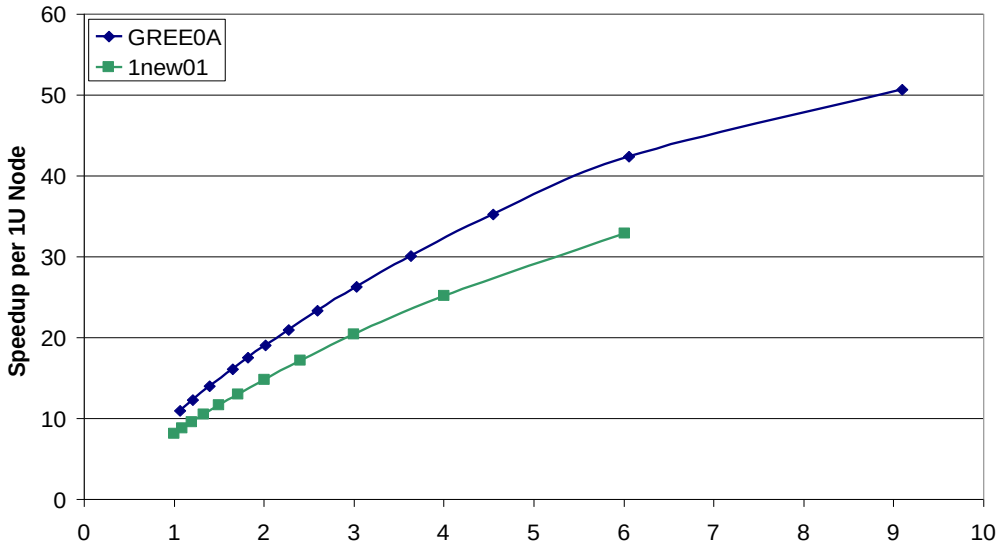
DOES NOT SCALE BEYOND 6 x86 CPU CORES



	Serial	2	4	6	8	12
HPBL460 g6 x5570 2.93Ghz	18986	11360	7606	5306	5466	
Westmere WSM A0 3.06Ghz default bios settings.	18697	11821	7665	5310	5552	5534
Westmere WSM A0 3.06Ghz C state switched off.	19043	11437	7691	5470	5649	5495
Westmere WSM B0 3.3 Ghz default bios settings.	17337	10942	6736	5083	5186	5250
Westmere WSM x5677 Supermicro	17150	10552	6858	4810	4981	

Schlumberger

MAXELER SOLUTION: 20-40x in 1U



Domain Specific Address and Data Encoding (*Patent Pending)

MAXELER Technologies