Vivado Build Timing Analysis TPA Tool

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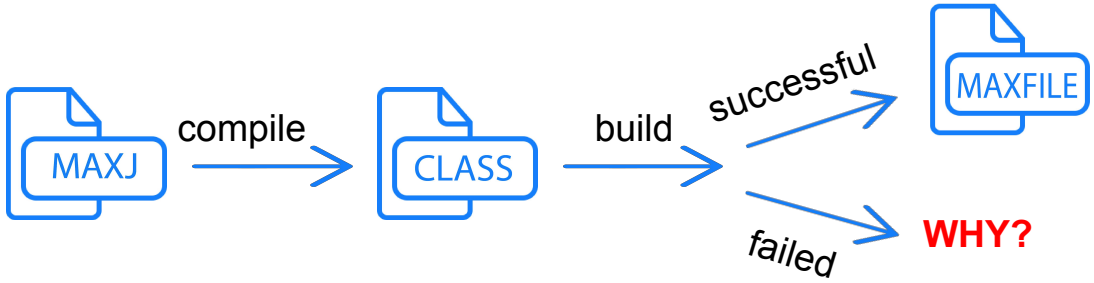
Building MaxJ Apps



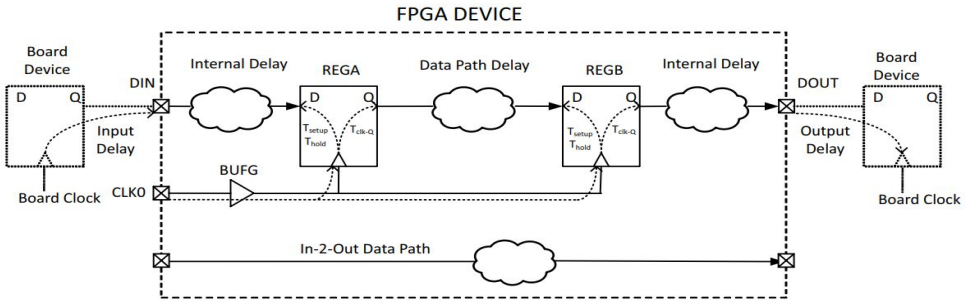
- Importance of figuring out why does the build fail
- Where to look? Vivado timing reports
- Timing reports are huge and not easy to understand

Possible problems on critical path:

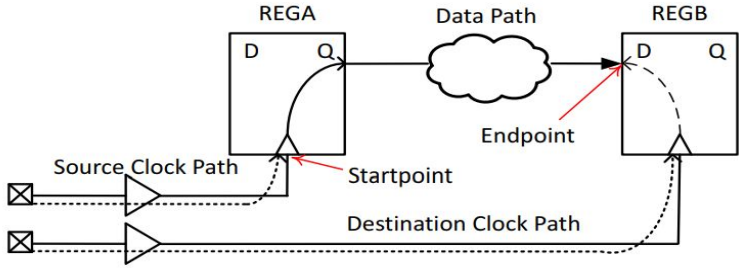
- Too many/few FFs
- Too big fanout
- Congestion

Possible solution:

- Create a tool to analyse and visualize timing reports



Timing Paths Example



Typical Timing Path

Reading a Timing Path Report

```
Slack (VIOLATED) :        -1.110ns  (required time - arrival time)
  Source:                 wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/m_sync_rx/g_on.g_single[0].m_sync/g_fd[1].m_fd/tamba_fd_synchronize_gray_r_reg/C
                            (rising edge-triggered cell FDRE clocked by clk_out2_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32  {rise@0.000n
  Destination:            wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_erx[0].m_erx/m_mrx/m_cp/te6c49u_IO0III_reg/D
                            (rising edge-triggered cell FDRE clocked by clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32  {rise@0.000n
  Path Group:             clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            3.103ns  (clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32 rise@3.103ns - clk_out2_com_maxeler_platform_max5
  Data Path Delay:        4.183ns  (logic 0.116ns (2.773%)  route 4.067ns (97.227%))
  Logic Levels:           1  (LUT6=1)
  Clock Path Skew:        0.727ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    8.443ns = ( 11.546 - 3.103 )
    Source Clock Delay      (SCD):    7.653ns
    Clock Pessimism Removal (CPR):    -0.063ns
  Clock Uncertainty:      0.199ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
      User System Jitter          :    0.050ns
    Discrete Jitter          (DJ):    0.141ns
    Phase Error              (PE):    0.120ns
  Inter-SLR Compensation: 0.583ns  ((DCD - CCD) * PF)
    Destination Clock Delay (DCD):    8.443ns
    Common Clock Delay      (CCD):    4.555ns
    Prorating Factor         (PF):    0.150
  Clock Net Delay (Source):      2.882ns (routing 0.964ns, distribution 1.918ns)
  Clock Net Delay (Destination): 3.649ns (routing 2.102ns, distribution 1.547ns)
```

Timing Path Summary Example

- Slack - positive slack indicates that the path meets the path requirement, which is derived from the timing constraints
- Source - path startpoint and the source clock that launches the data
- Destination - path endpoint and the destination clock that captures the data
- Requirement - timing path requirement
- Data Path Delay - accumulated delay through the logic section of the path
- Logic Levels - number of each type of primitives included in the data section of the path
- Clock Path Skew - insertion delay difference between the launch edge of the source clock and the capture edge of the destination clock
- Clock Uncertainty - total amount of possible time variation between any pair of clock edges

Reading a Timing Path Report

The second half of the report provides more details on the cells, pins, ports and nets traversed by the path. It is separated into three sections:

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock clk_out2_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32 rise edge)			
		0.000	0.000 r	
GTYE4_COMMON_X1Y14		0.000	0.000 r	gtrefclk_p_QSFP0 (IN)
	net (fo=0)	0.000	0.000	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/gtrefclk_p_QSFP0
GTYE4_COMMON_X1Y14	IBUFDS_GTE4 (Prop_IBUFDS0_GTYE4_GTYE4_COMMON_I_ODIV2)			
		0.408	0.408 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/IBUFDS_GTE4_inst/ODIV2
	net (fo=2, routed)	0.086	0.494	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/ODIV2
BUFG_GT_X1Y340	BUFG_GT (Prop_BUFG_GT_I_O)			
		0.130	0.624 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/bufg_gt_tx/O
	net (fo=1, routed)	3.995	4.619	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx/inst/clk_in1
SLR Crossing[2->1]				
MMCM_X0Y5	MMCME4_ADV (Prop_MMCM_CLKIN1_CLKOUT1)			
		-0.127	4.492 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx/inst/mmcme4_adv_inst/CLKOUT1
	net (fo=1, routed)	0.251	4.743	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx_n_1
BUFGCE_X0Y120	BUFGCE (Prop_BUFCE_BUFGCE_I_O)			
		0.028	4.771 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/bufg_tx_div2/O
X2Y8 (CLOCK_ROOT)	net (fo=26243, routed)	2.784	7.555	wrapper/wrapper_entity/Stream_76/inst_ln31_streamingblock/inst_ln78_portablecomponentsupplier/fifo/xpm_fifo_base_inst/gen_sdpram.xpm_memory_base_inst/clka
RAMB36_X9Y103	RAMB36E2		r	wrapper/wrapper_entity/Stream_76/inst_ln31_streamingblock/inst_ln78_portablecomponentsupplier/fifo/xpm_fifo_base_inst/gen_sdpram.xpm_memory_base_inst/gen_wr_a.gen_wc
RAMB36_X9Y103	RAMB36E2 (Prop_RAMB36E2_RAMB36_CLKARDCLK_DOUTADOUT[0])			
		0.830	8.385 f	wrapper/wrapper_entity/Stream_76/inst_ln31_streamingblock/inst_ln78_portablecomponentsupplier/fifo/xpm_fifo_base_inst/gen_sdpram.xpm_memory_base_inst/gen_wr_a.gen_w
	net (fo=7, routed)	0.684	9.069	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_cp/m_cb/tx_ull_eop_0
SLICE_X140Y517	LUT6 (Prop_G6LUT_SLICEL_I3_O)			
		0.089	9.158 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_cp/m_cb/te6c49u_OOOOlI[5]_i_3/O
	net (fo=2, routed)	0.310	9.468	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_cp/m_cb/p_26_in
SLICE_X140Y517	LUT6 (Prop_H6LUT_SLICEL_I1_O)			
		0.150	9.618 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_cp/m_cb/te6c49u_OOOOlI[5]_i_1__0/O
	net (fo=5, routed)	1.951	11.569	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_dp/m_df/te6c49u_lIO01[0].te6c49u_l1I0l/te6c49u_IlI0lI.m_ctrl/reg_ln434_stre
SLICE_X141Y516	FDRE		r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_dp/m_df/te6c49u_lIO01[0].te6c49u_l1I0l/te6c49u_IlI0lI.m_ctrl/te6c49u_OOOOlI
	(clock clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32 rise edge)			
		3.103	3.103 r	
GTYE4_COMMON_X1Y14		0.000	3.103 r	gtrefclk_p_QSFP0 (IN)
	net (fo=0)	0.000	3.103	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/gtrefclk_p_QSFP0
GTYE4_COMMON_X1Y14	IBUFDS_GTE4 (Prop_IBUFDS0_GTYE4_GTYE4_COMMON_I_ODIV2)			
		0.133	3.236 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/IBUFDS_GTE4_inst/ODIV2
	net (fo=2, routed)	0.078	3.314	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/ODIV2
BUFG_GT_X1Y340	BUFG_GT (Prop_BUFG_GT_I_O)			
		0.114	3.428 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/bufg_gt_tx/O
	net (fo=1, routed)	3.600	7.028	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx/inst/clk_in1
SLR Crossing[2->1]				
MMCM_X0Y5	MMCME4_ADV (Prop_MMCM_CLKIN1_CLKOUT0)			
		0.630	7.658 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx/inst/mmcme4_adv_inst/CLKOUT0
	net (fo=1, routed)	0.215	7.873	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx_n_0
BUFGCE_X0Y129	BUFGCE (Prop_BUFCE_BUFGCE_I_O)			
		0.024	7.897 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/bufg_tx/O
X4Y11 (CLOCK_ROOT)	net (fo=1997, routed)	3.399	11.296	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_dp/m_df/te6c49u_lIO01[0].te6c49u_l1I0l/te6c49u_IlI0lI.m_ctrl/bbstub_clk_out
SLICE_X141Y516	FDRE		r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_dp/m_df/te6c49u_lIO01[0].te6c49u_l1I0l/te6c49u_IlI0lI.m_ctrl/te6c49u_OOOOlI
	clock pessimism	-0.063	11.233	
	clock uncertainty	-0.199	11.034	
SLICE_X141Y516	FDRE (Setup_DFF2_SLICEM_C_CE)			
		-0.060	10.974	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_dp/m_df/te6c49u_lIO01[0].te6c49u_l1I0l/te6c49u_IlI0lI.m_ctrl/te6c49u_OOOOlI
	required time		10.974	
	arrival time		-11.569	
	slack		-0.595	

Source Clock Path

Data Path

Destination Clock Path

TPA Tool Output

- Two types of output -> json and txt
- Both contain details of all critical paths for app for each implementation strategy that was run

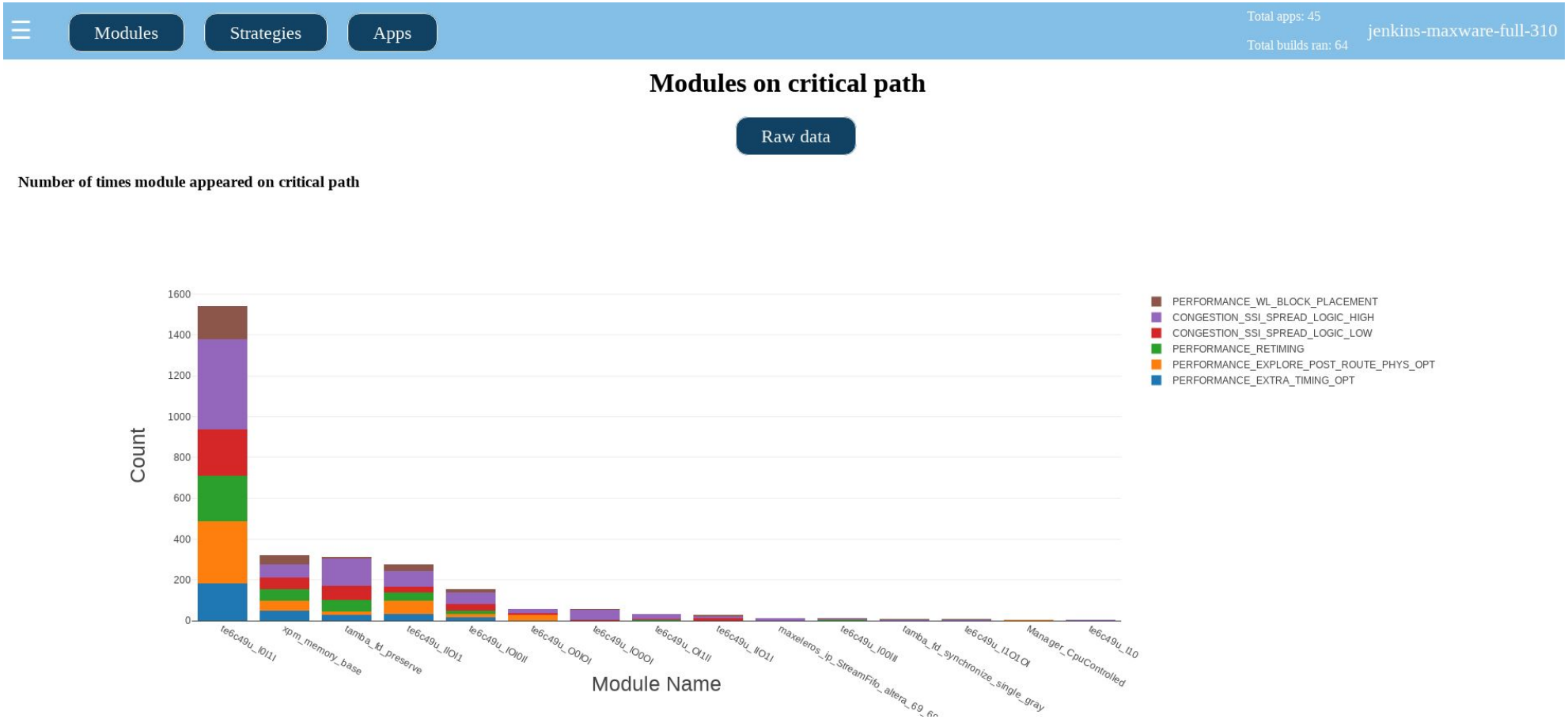
```
Delay Path 4
    Slack: -0.631
    Hierarchy root: wrapper/wrapper_entity/mcp2/
    Source: inst_ln168_statemachineentitycore/state3_write_data_buffer_valid_2_300MHz_reg[0]/C/
    Destination: inst_ln50_sourcefile5/U0/inst_fifo_gen/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg.gbmga.ngecc.bmg/inst_blk_mem_gen/gnbram.gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[2].ram.r/pri
    Data Path:
        Component type  | Delay Type                          | Delay (ns) | Resource
        ----------------------------------------------------------------------------
        | FDRE            Prop_HFF_SLICEL_C_Q                     0.082       inst_ln168_statemachineentitycore/state3_write_data_buffer_valid_2_300MHz_reg[0]/Q/
        | net             fo=9                                    0.746       inst_ln168_statemachineentitycore/state3_write_data_buffer_valid_2_300MHz_reg_n_0_[0]/
        | LUT6            Prop_A6LUT_SLICEL_I3_O                  0.15        inst_ln168_statemachineentitycore/inst_ln50_sourcefile_i_1613__0/O/
        | net             fo=1                                    0.088       inst_ln168_statemachineentitycore/inst_ln50_sourcefile_i_1613__0_n_0/
        | LUT6            Prop_G6LUT_SLICEL_I5_O                  0.084       inst_ln168_statemachineentitycore/inst_ln50_sourcefile_i_1069__1/O/
        | net             fo=8                                    0.15        inst_ln168_statemachineentitycore/assignableVar7/
        | LUT6            Prop_B6LUT_SLICEL_I5_O                  0.125       inst_ln168_statemachineentitycore/inst_ln50_sourcefile_i_1062__1/O/
        | net             fo=0                                    0.0         IBUFDS_freerunClk_inst/I/
        | IBUFCTRL        Prop_IBUFCTRL_HPIOB_M_I_O               0.0         IBUFDS_freerunClk_inst/IBUFCTRL_INST/O/
        | net             fo=1                                    0.496       O/
        | BUFGCE          Prop_BUFCE_BUFGCE_I_O                   0.021       BUFG_freerunClk_inst/O/
        | net             fo=7                                    3.112       stream4_clock_gen_i/input_clock_sig/
        | BUFGCE          Prop_BUFCE_BUFGCE_I_O                   0.021       stream4_clock_gen_i/mmcm_clkout0_300B_BUFG_inst/O/
        | net             fo=0                                    0.0         IBUFDS_freerunClk_inst/I/
        | IBUFCTRL        Prop_IBUFCTRL_HPIOB_M_I_O               0.0         IBUFDS_freerunClk_inst/IBUFCTRL_INST/O/
        | net             fo=1                                    0.579       O/
        | BUFGCE          Prop_BUFCE_BUFGCE_I_O                   0.024       BUFG_freerunClk_inst/O/
        | net             fo=7                                    3.41        stream4_clock_gen_i/input_clock_sig/
        | BUFGCE          Prop_BUFCE_BUFGCE_I_O                   0.024       stream4_clock_gen_i/mmcm_clkout0_300B_BUFG_inst/O/
        | net             fo=8029                                 3.42        mcp0/inst_ln168_statemachineentitycore/freerun_clk_n/
```

From txt report developers can see:

- All critical paths sorted by slack
- All components on each critical path
- Fanout for each component and how much does it affect delay time

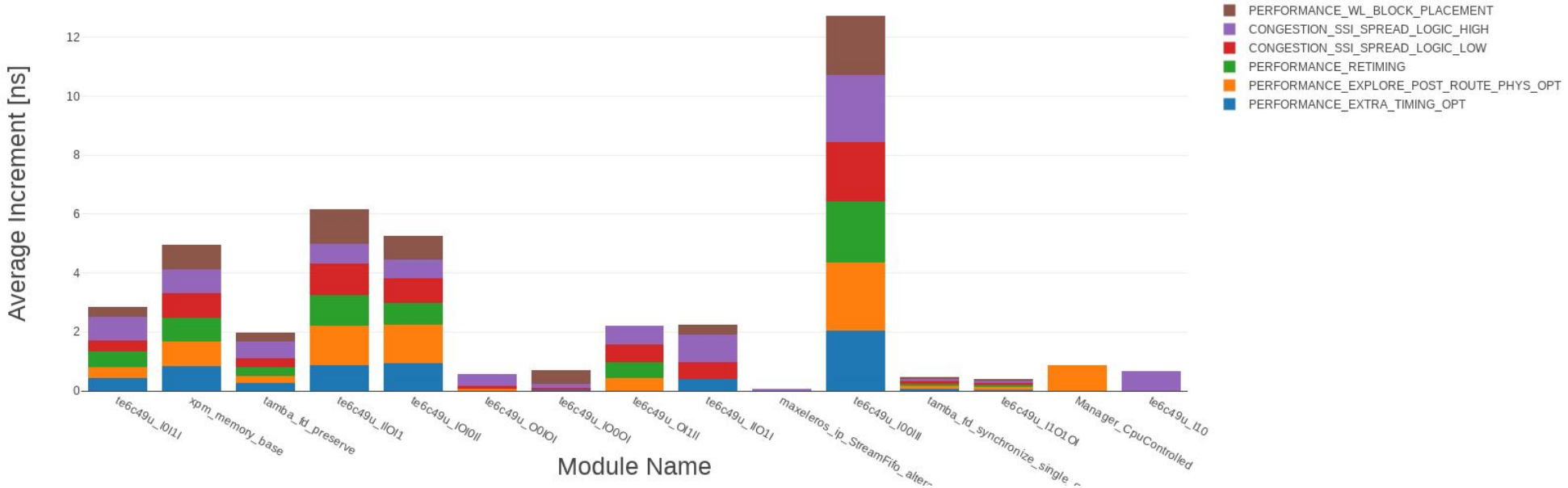
TPA on Maxware Builds - Modules View

- Running TPA tool on multiple builds
- Visualize data as interactive html report
- All data is available in json format -> users can write their own visualization scripts

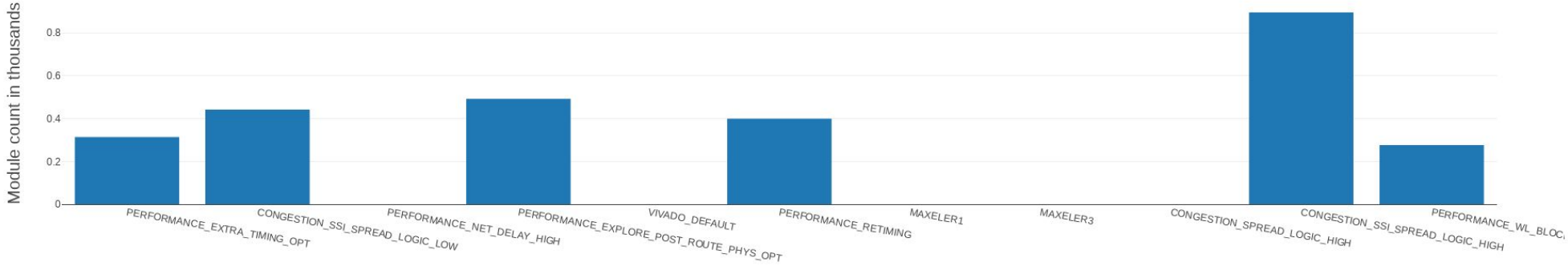


Number of Times Module Appeared on Critical Path for Each Strategy

TPA on Maxware Builds - Modules View

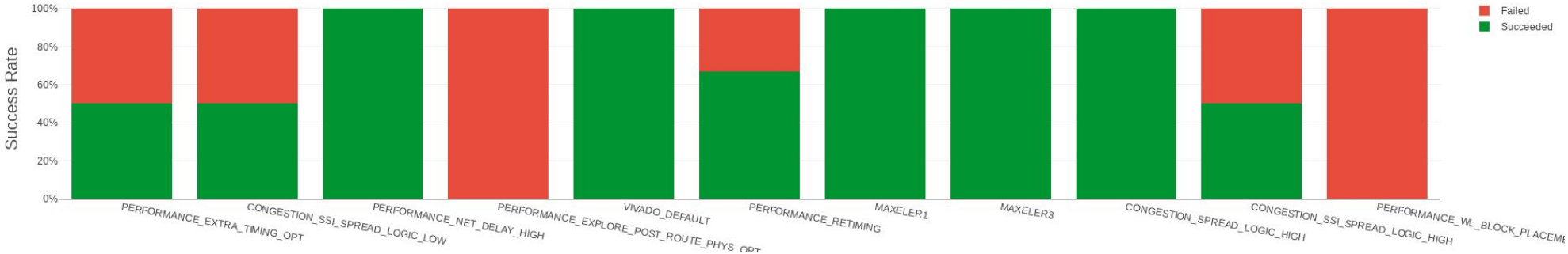


Average Increment for Each Module on Critical Path Per Strategy

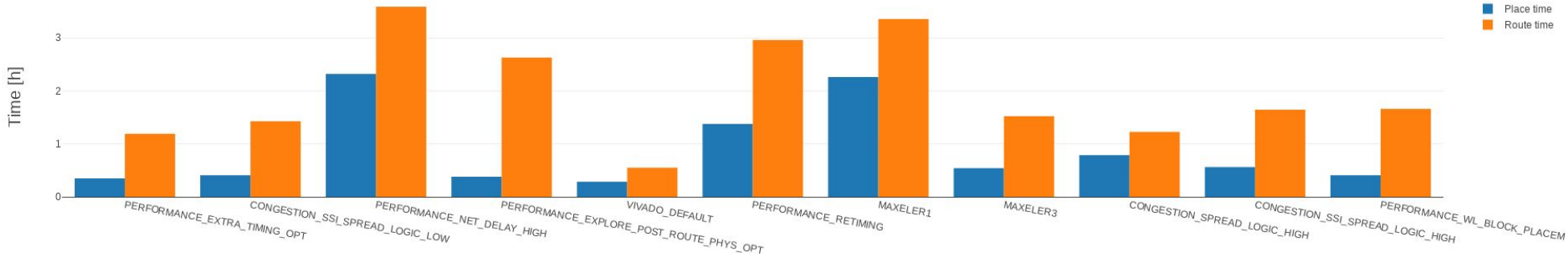


Module Count on Critical Path for Each Strategy

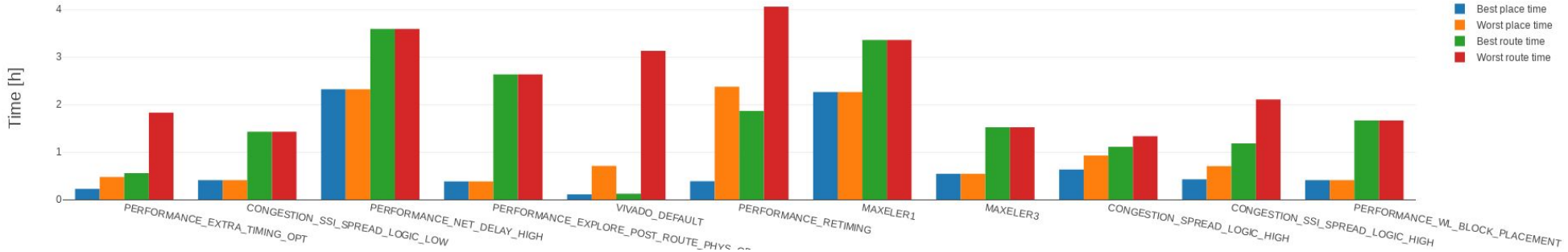
TPA on Maxware Builds - Strategies View



Success/failure percentage per strategy



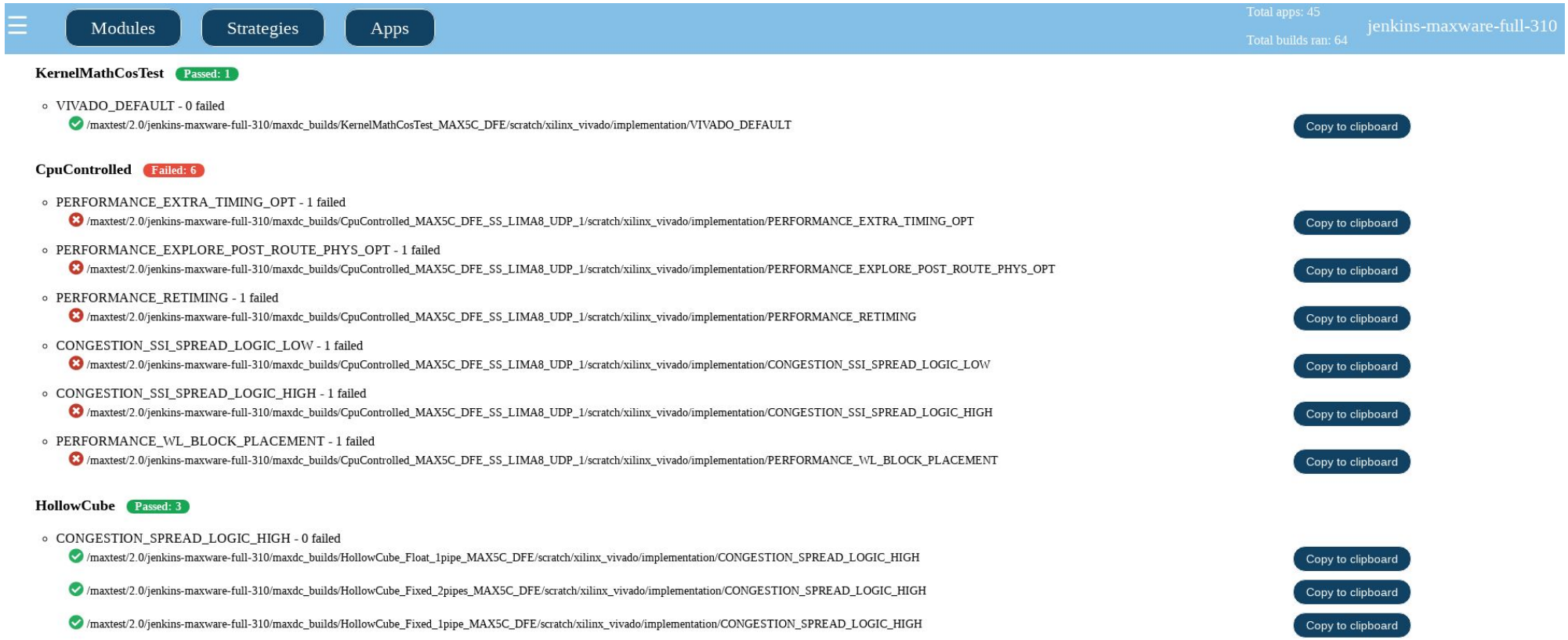
Average place and route time per strategy



Best and worst place/route time per strategy

TPA on Maxware Builds - Apps View

- Detailed overview of all apps built with all engine parameters and path to build locations.
- Work in progress.



List of all apps that were part of the Maxware build

Future Improvements

- Integrate txt output in MaxIDE
- Make it part of Maxware build CI job
- Add separate report for each app
- Add more explanation (legend maybe) for all elements shown in txt format
- Add analysis for Min delay paths (hold/removal)
- Investigate how is the build affected by: enables, clock skew, clock tree
- Create a list of top 10 critical apps in Maxeler with every new compiler release and use them to improve compiler