Vivado Build Timing Analysis **TPA Tool**

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MAXIMUM PERFORMANCE COMPUTING

Building MaxJ Apps



- Importance of figuring out why does the build fail
- Where to look? Vivado timing reports
- Timing reports are huge and not easy to understand

Possible problems on critical path:

- Too many/few FFs
- Too big fanout
- Congestion

Possible solution:

• Create a tool to analyse and visualize timing reports





Reading a Timing Path Report

Slack (VIOLATED) :	-1.110ns (required time - arrival time)
Source:	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/m_sync_rx/g_on.g_single[0].m_sync/g_fd[1].m_fd/tamba_fd_synchronize_gray_r_reg/C
	(rising edge-triggered cell FDRE clocked by clk_out2_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32 {rise@0.000n
Destination:	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_erx[0].m_erx/m_mrx/m_cp/te6c49u_I00III_reg/D
	(rising edge-triggered cell FDRE clocked by clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32 {rise@0.000n
Path Group:	clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32
Path Type:	Setup (Max at Slow Process Corner)
Requirement:	3.103ns (clk_out1_com_maxeler_platform_max5_toolchain_ip_clockingwizard_UllMmcm_vivado2017_4_xcVU9P_FLGB2104_2_E_xusp_mmcm_m66_d32 rise@3.103ns - clk_out2_com_maxeler_platform_max5
Data Path Delay:	4.183ns (logic 0.116ns (2.773%) route 4.067ns (97.227%))
Logic Levels:	1 (LUT6=1)
Clock Path Skew:	0.727ns (DCD - SCD + CPR)
Destination Clock Del	Lay (DCD): 8.443ns = (11.546 - 3.103)
Source Clock Delay	(SCD): 7.653ns
Clock Pessimism Remov	/al (CPR): -0.063ns
Clock Uncertainty:	0.199ns ((TSJ^2 + DJ^2)^1/2) / 2 + PE
Total System Jitter	(TSJ): 0.071ns
User System Jitter	: 0.050ns
Discrete Jitter	(DJ): 0.141ns
Phase Error	(PE): 0.120ns
Inter-SLR Compensation:	: 0.583ns ((DCD - CCD) * PF)
Destination Clock Del	Lay (DCD): 8.443ns
Common Clock Delay	(CCD): 4.555ns
Prorating Factor	(PF): 0.150
Clock Net Delay (Source	e): 2.882ns (routing 0.964ns, distribution 1.918ns)
Clock Net Delay (Destin	nation): 3.649ns (routing 2.102ns, distribution 1.547ns)

Timing Path Summary Example

- Slack positive slack indicates that the path meets the path requirement, which is derived from the timing constraints
- Source path startpoint and the source clock that launches the data
- Destination path endpoint and the destination clock that captures the data
- Requirement timing path requirement
- Data Path Delay accumulated delay through the logic section of the path
- Logic Levels number of each type of primitives included in the data section of the path
- Clock Path Skew insertion delay difference between the launch edge of the source clock and the capture edge of the destination clock
- Clock Uncertainty total amount of possible time variation between any pair of clock edges

Reading a Timing Path Report

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The second half of the report provides more details on the cells, pins, ports and nets traversed by the path. It is separated into three sections:

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock clk out2 com maxele	er platfor	m max5 tool	chain ip clockingwizard UllMmcm vivado2017 4 xcVU9P FLGB2104 2 E xusp mmcm m66 d32 rise edge)
		0.000	0.000 r	
GTYE4_COMMON_X1Y14	net (fe-0)	0.000	0.000 r	gtrefclk_p_QSFP0 (IN) yrannar (Natyrek 6550 (ull 10g athornat subayatam yrannar/atrafalk a 05500
GTYE4 COMMON X1Y14	IBUFDS GTE4 (Prop IBUFDS0	GTYE4 GTYI	E4 COMMON I	wrapper/metwork_vsrro/utc_tog_ethernet_subsystem_wrapper/gtrefctk_p_tsrro
		0.408	0.408 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/IBUFDS_GTE4_inst/ODIV2
	net (fo=2, routed)	0.086	0.494	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/ODIV2
BUFG_GT_X1Y340	BUFG_GI (Prop_BUFG_GI_1_0)	6 136	0.624 r	wranner/Natwork OSEP0/ull 10g athernat subsystem wranner/bufg at tv/O
	net (fo=1, routed)	3.995	4.619	wrapper/metwork_vsrro/utc_tog_ethernet_subsystem_nrapper/bdrg_gtx/o
SLR Crossing[2->1]				
MMCM_X0Y5	MMCME4_ADV (Prop_MMCM_CLKI	N1_CLKOUT	1)	
	net (fo=1 routed)	0.127	4.492 r 4 743	Wrapper/Network_USFP0/ull_10g_etnernet_subsystem_wrapper/mmcm_tx/inst/mmcme4_adv_inst/LLKUUI1 wranner/Network_DSFP0/ull_10g_etnernet_subsystem_wranner/wrmcmt tx_n_l
BUFGCE X0Y120	BUFGCE (Prop BUFCE BUFGCE	I 0)	4.745	n abbet the energy of the state
		0.028	4.771 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/bufg_tx_div2/0
X2Y8 (CLOCK_ROOT)	net (fo=26243, routed)	2.784	7.555	wrapper/wrapper_entity/Stream_76/inst_ln31_streamingblock/inst_ln78_portablecomponentsupplier/fifo/xpm_fifo_base_inst/gen_sdpram.xpm_memory_base_inst/clka
KAMB30_X91103	KAMB36E2			wrapper/wrapper_entity/stream_/o/inst_thsi_streamingolock/inst_th/8_portablecomponentsupplier/fifo/xpm_fito_base_inst/gen_supram.xpm_memory_base_inst/gen_wr_a.gen_wr
RAMB36_X9Y103	RAMB36E2 (Prop_RAMB36E2_RA	MB36_CLKA	RDCLK_DOUTA	DOUT[0])
		0.830	8.385 f	wrapper/wrapper_entity/Stream_76/inst_ln31_streamingblock/inst_ln78_portablecomponentsupplier/fifo/xpm_fifo_base_inst/gen_sdpram.xpm_memory_base_inst/gen_wr_a.gen_w
	INTE (Prop GELUT SITCEL T	0.684	9.069	wrapper/Network_VSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx10].m_etx/m_mtx/m_cp/m_cb/tx_ull_eop_0
SEICE_X1401317		0.089	9.158 r	wrapper/Network 05FP0/ull 10g ethernet subsystem wrapper/i ullmac/g etx[0].m etx/m mtx/m cp/m cb/te6c49u 0000ll[5] i 3/0 Data Path
	net (fo=2, routed)	0.310	9.468	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_cp/m_cb/p_26_in
SLICE_X140Y517	LUT6 (Prop_H6LUT_SLICEL_I]	_0)		
	net (fe_5_routed)	0.150	9.618 r	wrapper/Network (SFP0/ull_10g_ethernet_subsystem_wrapper/1_ullmac/g_etx[0].m_etx/m_mtx/m_cp/m_cb/te6c49u_00001[15]_10/0
SLICE X141Y516	FDRE	1.951	11.309 r	wrapper/metwork_vsrFo/utc_tog_ethernet_subsystem_wrapper/l_itcmad/g_etxt0.m_etx/m_mix/m_up/m_in/teotesu_citooing/teotesu_citooing/teotesu_citooing/teotesu_citooing/teotesu_citooing/teotesu_citooing/teotesuciton
	[[]] and all out] com movels	e elstfor		
	(CLOCK CLK_OUT1_COM_MAXELE	r_platfor	m_max5_tool 3 103 r	chain_lp_clockingwizard_ullMmcm_vivadozui/_4_xcvuyP_FLGB2104_zE_xusp_mmcm_mob_d32 fise edge)
GTYE4_COMMON_X1Y14		0.000	3.103 r	gtrefclk_p_QSFP0 (IN)
	net (fo=0)	0.000	3.103	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/gtrefclk_p_QSFP0
GTYE4_COMMON_X1Y14	IBUFDS_GTE4 (Prop_IBUFDS0_	GTYE4_GTY	E4_COMMON_I	
	net (fo=2, routed)	0.133	3.230 1	wrapper/metwork_vspro/utt_tog_ethernet_subsystem_wrapper/100/vs_uste_inst/00/v2 Uestination Clock Pain
BUFG_GT_X1Y340	BUFG_GT (Prop_BUFG_GT_I_0)			
		0.114	3.428 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/bufg_gt_tx/0
CLD Crossing[2 > 1]	net (fo=1, routed)	3.600	7.028	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx/inst/clk_inl
MMCM X0Y5	MMCME4 ADV (Prop MMCM CLK)	N1 CLKOUT	9)	
		0.630	7.658 r	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx/inst/mmcme4_adv_inst/CLKOUT0
	net (fo=1, routed)	0.215	7.873	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/mmcm_tx_n_0
BUFGCE_X0Y129	BUFGCE (Prop_BUFCE_BUFGCE_	I_0)	7 007 -	VERDER / Meturek ASE80/ull 10g atherent autoveram versener/bufg tv/0
X4Y11 (CLOCK BOOT)	net (fo=1997, routed)	3.399	11.296	wrapper/metwork_gsrrorutc_tog_ethernet_subsystem_wrapper/burg_tXy ullmac/g etx[0].m etx/m mtx/m dp/m df/te6c49u]1001[0].te6c49u]1101/te6c49u]1101/te6c49u]1101/te6c49u]1101/te6c49u]101/te6c49u]101/te
SLICE_X141Y516	FDRE	0.000	r 11.1200	wrapper/Network_QSFP0/ull_10g_ethernet_subsystem_wrapper/i_ullmac/g_etx[0].m_etx/m_mtx/m_dp/m_df/te6c49u_l1001[0].te6c49u_l1101/te6c49u_l1101.m_ctrl/te6c49u_0000l1
	clock pessimism	-0.063	11.233	
	clock uncertainty	-0.199	11.034	
SEICE_X1411516	FURE (Setup_DFF2_SLICEM_C_	-0.060	10,974	wrapper/Network 05FP0/ull 10g ethernet subsystem wrapper/i ullmac/g etx[0],m etx/m mtx/m dp/m df/te6c49u 11001[0].te6c49u 11101/te6c49u 11101] m ctrl/te6c49u 00001T
	required time		10.974	
	arrival time		-11.569	
	slack		-0.595	

TPA Tool Output

- Two types of output -> json and txt
- Both contain details of all critical paths for app for each implementation strategy that was run

36 37 38 39 40 41 42	Delay Path Slack: Hieran Source Destir Data F	h 4 : -0.631 rchy root: wrap e: inst_ln168_s nation: inst_ln Path: omponent type	per/wrapper_entity/mcp2/ tatemachineentitycore/state3_write_d 50_sourcefile5/U0/inst_fifo_gen/gcon Delay Type	ata_buffer_valid_2_300 vfifo.rf/grf.rf/gntv_c Delay (ns)	MHz_reg[0]/C/ r_sync_fifo.mem/gbm.gbmg.gbmga.ngecc.bmg/inst_blk_mem_gen/gnbram.gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[2].ram.r/pri Resource
43 44		FDRF	Prop HEE SLICEL C 0	0.082	inst ln168 statemachineentitycore/state3 write data buffer valid 2 300MHz reg[0]/0/
45		net	fo=9	0.746	inst lni68 statemachineentitycore/state3 write data buffer valid 2 300MHz reg n 0 [0]/
46		LUT6	Prop A6LUT SLICEL I3 0	0.15	inst ln168 statemachineentitycore/inst ln50 sourcefile i 1613 0/0/
47		net	fo=1	0.088	inst ln168 statemachineentitycore/inst ln50 sourcefile i 1613 0 n 0/
48		LUT6	Prop_G6LUT_SLICEL_I5_0	0.084	inst ln168 statemachineentitycore/inst ln50 sourcefile i 1069 1/0/
49		net	fo=8	0.15	inst_ln168_statemachineentitycore/assignableVar7/
50		LUT6	Prop_B6LUT_SLICEL_I5_0	0.125	inst_ln168_statemachineentitycore/inst_ln50_sourcefile_i_10621/0/
51		net	fo=0	0.0	IBUFDS_freerunClk_inst/I/
52		IBUFCTRL	<pre>Prop_IBUFCTRL_HPI0B_M_I_0</pre>	0.0	IBUFDS_freerunClk_inst/IBUFCTRL_INST/0/
53		net	fo=1	0.496	0/
54		BUFGCE	<pre>Prop_BUFCE_BUFGCE_I_0</pre>	0.021	BUFG_freerunClk_inst/0/
55		net	fo=7	3.112	<pre>stream4_clock_gen_i/input_clock_sig/</pre>
56		BUFGCE	<pre>Prop_BUFCE_BUFGCE_I_0</pre>	0.021	stream4_clock_gen_i/mmcm_clkout0_300B_BUFG_inst/0/
57		net	fo=0	0.0	IBUFDS_freerunClk_inst/I/
58		IBUFCTRL	<pre>Prop_IBUFCTRL_HPIOB_M_I_0</pre>	0.0	IBUFDS_freerunClk_inst/IBUFCTRL_INST/0/
59		net	fo=1	0.579	0/
60		BUFGCE	<pre>Prop_BUFCE_BUFGCE_I_0</pre>	0.024	BUFG_freerunClk_inst/0/
61		net	fo=7	3.41	stream4_clock_gen_i/input_clock_sig/
62		BUFGCE	Prop_BUFCE_BUFGCE_I_0	0.024	stream4_clock_gen_i/mmcm_clkout0_300B_BUFG_inst/0/
63		net	fo=8029	3.42	mcp0/inst_ln168_statemachineentitycore/freerun_clk_n/
64					

From txt report developers can see:

- All critical paths sorted by slack
- All components on each critical path
- Fanout for each component and how much does it affect delay time

TPA on Maxware Builds - Modules View

- Running TPA tool on multiple builds
- Visualize data as interactive html report
- All data is available in json format -> users can write their own visualization scripts

Module	s	Strategies Apps	Total apps: 45 Total builds ran: 64	jenkins-maxware-full-31
		Modules on critical path		
		Raw data		
Number of times m	odule apj	peared on critical path		
	1600			ICNIT.
	1400		CONGESTION_SSI_SPREAD_LOGIC_H CONGESTION_SSI_SPREAD_LOGIC_L	ligh OW
	1200		PERFORMANCE_RETINING PERFORMANCE_EXPLORE_POST_RC PERFORMANCE_EXTRA_TIMING_OPT	UTE_PHYS_OPT
t	1000			
Cou	800			
	600			
	200			
	0_	1660 1000 1000 1000 1000 1000 1000 1000		
		- "I'GU_ IO[1] - "I'GU_ IO[2] - "I'G		
		Would runne dea 60 60 60 000		

Number of Times Module Appeared on Critical Path for Each Strategy



TPA on Maxware Builds - Modules View



Module Count on Critical Path for Each Strategy



TPA on Maxware Builds - Strategies View



Success/failure percentage per strategy



Average place and route time per strategy



Best and worst place/route time per strategy

MAXELER

Technologies

3H PARTNERS

TPA on Maxware Builds - Apps View

- Detailed overview of all apps built with all engine parameters and path to build locations.
- Work in progress.

E Modules Strategies Apps	Total apps: 45 jenkins-maxware-full-310 Total builds ran: 64
KernelMathCosTest Passed: 1	
 VIVADO_DEFAULT - 0 failed /maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/KernelMathCosTest_MAX5C_DFE/scratch/xilinx_vivado/implementation/VIVADO_DEFAULT 	Copy to clipboard
CpuControlled Failed: 6	
 PERFORMANCE_EXTRA_TIMING_OPT - 1 failed (%) /maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/CpuControlled_MAX5C_DFE_SS_LIMA8_UDP_1/scratch/xilinx_vivado/implementation/PERFORMANCE_EXTRA_TIMING_OPT 	Copy to clipboard
 PERFORMANCE_EXPLORE_POST_ROUTE_PHYS_OPT - 1 failed (maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/CpuControlled_MAX5C_DFE_SS_LIMA8_UDP_1/scratch/xilinx_vivado/implementation/PERFORMANCE_EXPLORE_POST_ROUTE_PHYS_OPT 	Copy to clipboard
 PERFORMANCE_RETIMING - 1 failed /maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/CpuControlled_MAX5C_DFE_SS_LIMA8_UDP_1/scratch/xilinx_vivado/implementation/PERFORMANCE_RETIMING 	Copy to clipboard
 CONGESTION_SSI_SPREAD_LOGIC_LOW - 1 failed (2.0/jenkins-maxware-full-310/maxdc_builds/CpuControlled_MAX5C_DFE_SS_LIMA8_UDP_1/scratch/xilinx_vivado/implementation/CONGESTION_SSI_SPREAD_LOGIC_LOW 	Copy to clipboard
 CONGESTION_SSI_SPREAD_LOGIC_HIGH - 1 failed (2.0/jenkins-maxware-full-310/maxdc_builds/CpuControlled_MAX5C_DFE_SS_LIMA8_UDP_1/scratch/xilinx_vivado/implementation/CONGESTION_SSI_SPREAD_LOGIC_HIGH 	Copy to clipboard
 PERFORMANCE_WL_BLOCK_PLACEMENT - 1 failed /maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/CpuControlled_MAX5C_DFE_SS_LIMA8_UDP_1/scratch/xilinx_vivado/implementation/PERFORMANCE_WL_BLOCK_PLACEMENT 	Copy to clipboard
HollowCube Passed: 3	
 CONGESTION_SPREAD_LOGIC_HIGH - 0 failed /maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/HollowCube_Float_1pipe_MAX5C_DFE/scratch/xilinx_vivado/implementation/CONGESTION_SPREAD_LOGIC_HIGH 	Copy to clipboard
Signation // Maxtest/2.0/jenkins-maxware-full-310/maxdc_builds/HollowCube_Fixed_2pipes_MAX5C_DFE/scratch/xilinx_vivado/implementation/CONGESTION_SPREAD_LOGIC_HIGH	Copy to clipboard
Similar Content of the content of th	Copy to clipboard

List of all apps that were part of the Maxware build



Future Improvements

- Integrate txt output in MaxIDE
- Make it part of Maxware build CI job
- Add separate report for each app
- Add more explanation (legend maybe) for all elements shown in txt format
- Add analysis for Min delay paths (hold/removal)
- Investigate how is the build affected by: enables, clock skew, clock tree
- Create a list of top 10 critical apps in Maxeler with every new compiler release and use them to improve compiler

