XF8279 Programmable Keyboard Display Interface

September 16, 1999 Product Specification

Memec Design Services

7810 South Hardy Drive, Suite 104
Tempe, Arizona 85284 USA
Phone: +1 888-845-5585 (USA)
+1 480-753-5585
Fax: +1 480-753-5899
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Features

- Compatible with Xilinx CORE Generator tool
- Simultaneous keyboard and display operations
- Scanned keyboard mode
- Scanned sensor mode
- Strobed input entry mode
- 8-character keyboard FIFO
- 2-key lockout or N-Key rollover with contact debounce
- Dual 4, 8, or 16 numerical display
- Single 8 or 16 character display
- Mode programmable from CPU
- Right or left entry 16-Byte display RAM
- Programmable scan timing
- Interrupt output on key entry

Applications

- User interface for embedded systems

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E/XL	Spartan
CLBs Used		
Core	183	183
Core+Ext logic	183	183
Core I/O		
Core[1]	49	49
Core+Ext logic	38	38
System Clock f_{max}	8 MHz[2]	
Device Features Used	RAM, OSC4, 3 BUFGs	
Provided with Core		
Documentation	User's guide, application notes, implementation instructions	
Design File Formats	.ngo netlist, Viewlogic source files available extra	
Constraint Files	.ucf	
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim, Testbench for VHDL and Verilog	
Symbols	Viewlogic, Foundation, Instantiation templates for VHDL and Verilog	
Evaluation Model	None	
Reference Designs & Application Notes	Sample designs in Viewlogic, Foundation, VHDL, and Verilog	
Additional Items	Warranty by MDS, Netlist only version available on enCORE CD-ROM	
Design Tool Requirements		
Xilinx Core Tools	Alliance/Foundation 1.4	
Support		
Support provided by Memec Design Services.		

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.

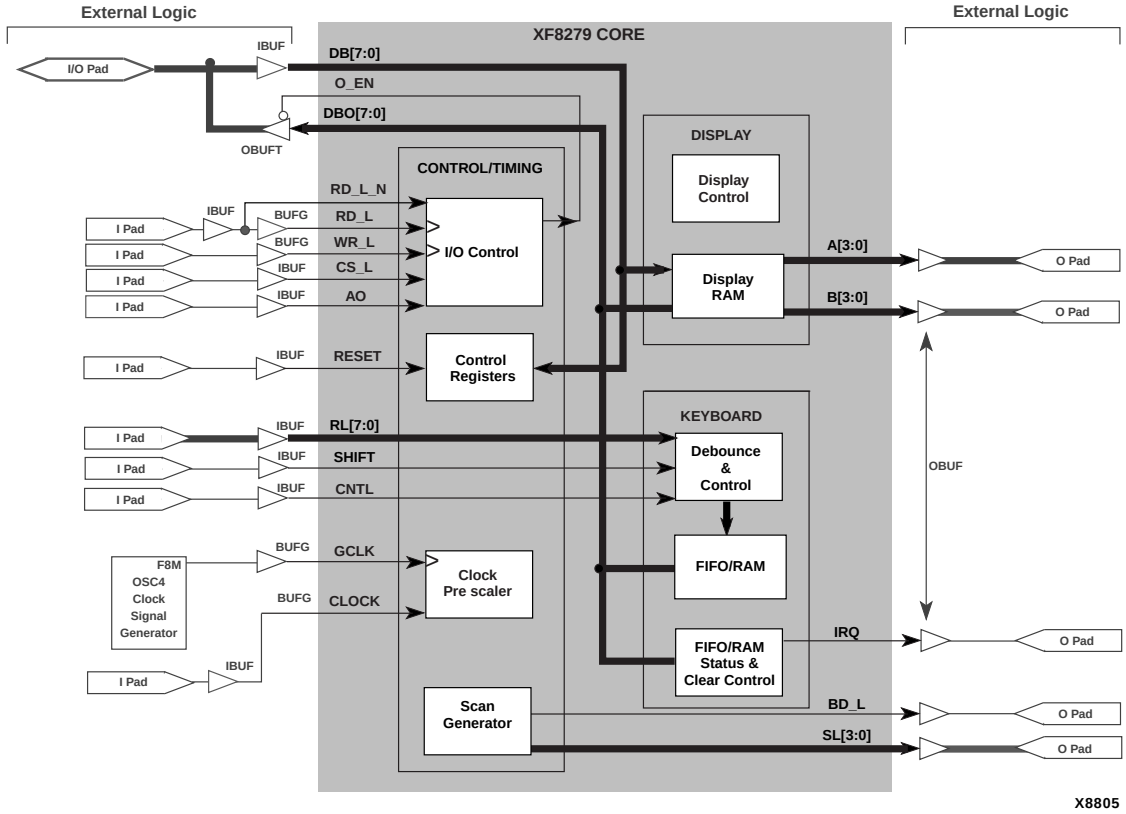

Figure 1: XF8279 Programmable Keyboard Display Interface Block Diagram

General Description

The XF8279 is a core logic module specifically designed for Xilinx FPGAs which emulates the functionality of the industry standard 8279 programmable keyboard and display interface. It facilitates upgrading current systems by allowing the designer to incorporate the 8279 function as well as other logic into a single, state of the art FPGA.

This core is designed such that it can be instantiated into a Xilinx design and hooked up to I/O buffers and pads, some BUFGs, and the 8 MHz OSC4 module and then compiled to make a device that will plug into an 8279 application.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The XF8279 has a 16 x 8 display RAM that can be organized into dual 16 x 4 RAMs. The RAM can be loaded or interrogated by the CPU. Both right entry calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto increment of the display RAM address.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, then run through a global buffer, then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core inor-

der to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

Functional Description

The XF8279 is partitioned into modules as shown in Figure 1 and described below. Refer to the XF8279 Programmable Keyboard Display Interface User's Guide for detailed technical information. The User's Guide is available, directly from MDS.

Control/Timing Group

The Control/Timing Group is comprised of the I/O Control, Control Registers, Clock Prescaler, and Scan Generator. This group establishes timing and controls the movement of data throughout the XF8279 core.

I/O Control

This block together with the external data bus buffers makes up the microprocessor interface. The 8-bit data output bus, DBO[7:0], provides data from the core during microprocessor read cycles. And the 8-bit input data bus, DB[7:0], provides data to the core during microprocessor write cycles. Typically, the Data Buffers are implemented with OBUFTs and IBUFs external to the core logic. The OBUFTs are enabled with an active low enable, O_EN, which is provided by the core during read cycles. It is simply a logical OR of RD_L and CS_L.

Write cycles to the core are performed with WR_L, CS_L, and A0. DB[7:0] and A0 are registered on the rising edge of WR_L only when CS_L is asserted (low). The level of A0 determines whether the core interprets the value on DB[7:0] as a command (A0=1) or as display data (A0=0). The registered signals are resynchronized with the free running 8MHz clock, GCLK, and the appropriate command is executed or display data written.

Read cycles from the core are performed with RD_L, CS_L, and A0. The falling edge of RD_L registers the state of A0 when CS_L is asserted (low). If A0 is sampled low, then, depending on the previous command, a value from either the keyboard FIFO/Sensor RAM or the display RAM is presented on the output data bus, DBO[7:0]. If A0 is sampled high, then the status word is presented on DBO[7:0].

Control Registers

Eight control registers can be written by the microprocessor using the command write cycles described above (A0=1). The eight registers are: Mode Set, Prescaler Divisor, FIFO/RAM Read Address, Display RAM Read Address, Display RAM Write Address, Display Write Mode, Clear, and EOI/Error Mode. A command write to some of these registers simply loads in a value, e.g. Prescaler Divisor. A command write to some other registers both loads in a value and performs a command, e.g. Display RAM Read Address.

Clock Prescalers

The Clock Prescaler divides the external system clock input, CLOCK, by a programmable divisor between 2 and 31 to generate an internal frequency of 100 kHz.

Scan Generator

The Scan Generator block further divides the output of the Clock Prescaler (nominally 100 kHz) by 64 and resynchronizes it with the internal 8 MHz clock to generate an internal scan clock enable of 1.56 kHz (640µs). This internal scan clock enable increments the scan counter itself which is simply a 4-bit binary counter. The least significant two bits of the counter are decoded to a 1 of 4 scan. A bit in the Mode Set register determines whether the counter outputs (encoded scan) or the decoder outputs (decoded scan) are output from the core on SL[3:0]. When using encoded scan, an external (to the core) 1 of 8 or 1 of 16 decoder is required. Note that both the keyboard matrix and the display use the same scan counter outputs. If the keyboard is in decoded scan, so is the display and therefore it will only display the first four characters in Display RAM.

This block also generates the display blanking signal, BD_L. This signal is asserted (low) around each transition of the scan counter to blank the display during digit switching.

Display Group

The Display Group consists of the Display Control block and the Display RAM block. Its function is to provide the display data to a multiplexed display synchronized with the Scan Generator. A mechanism is provided to clear the RAM and to allow the host microprocessor to independently write to either the upper or lower 4-bit nibbles.

Display Control

The Display Control block controls all data flow into and out of the Display RAM. Two counters provide the Display RAM address: the Read/Write address counter and the Display address counter.

The Read/Write address counter is loaded when the host microprocessor writes to either the Display RAM Read Address or the Display RAM Write Address command register. A subsequent data read or write (A0=0) by the host microprocessor will be to and from the RAM address held in the counter. If the auto increment feature is enabled, the address will increment automatically after the read or write cycle, thereby, relieving the host microprocessor from writing a display RAM address command for each access. In addition, the write enables to the upper and lower nibbles of the Display RAM can be disabled independently, allowing the host microprocessor to write display data on nibble boundaries.

The Display address counter steps through the Display RAM as the scan counter is incremented, providing charac-

ter data to the multiplexed display. This counter cycles through 16, 8, or 4 addresses depending on whether the display mode is set for 16 or 8 characters or if decoded scanning is enabled. The auto increment and right/left entry modes adjust this counter with respect to the scan counter.

The Display Control block also contains the clear display logic. The host microprocessor can write a code to the Clear command register to initiate the Display RAM clear logic. Depending on the code, the Display RAM will be filled with all 1's, all 0's or the constant 0x20. This logic uses the Read/Write address counter to access the RAM.

Display RAM

The Display RAM block consists of a 16 x 8 RAM organized as two 16 x 4 RAMs with common address inputs but separate write enable inputs. The Display Control block provides the address, write enables, and inputs data.

Keyboard Group

The Keyboard Group is comprised of the Debounce and Control block, the FIFO/RAM block, and the FIFO/RAM Status and Clear Control block. This group performs all input operations related to the return line inputs, RL[7:0].

Debounce and Control

The input data comes into the core through the 8 return lines, RL[7:0], and since these inputs are considered active low, each bit is inverted. For scanned input modes (keyboard or sensor matrix), the return lines are registered at the end of each scan counter state.

In keyboard modes only, the inputs are debounced by comparing the current registered input with the value that was registered 1 complete scan cycle ago (8 scan counts for encoded scanning and 4 scan counts for decoded scanning). If a switch remains closed for two consecutive scan cycles and it had been open for two consecutive scan cycles before that, the current scan count, the number of the active return line, the state of the CNTL and SHIFT inputs are all pushed into the FIFO.

In sensor matrix mode, no debounce is performed and the registered input is written into the FIFO/RAM at the address specified by the current scan count. The FIFO/RAM is written with new input data every scan count.

In strobed input mode, the value of the inverted return lines is pushed into the FIFO on the rising edge of the CNTL input.

FIFO/RAM

The FIFO/RAM operates as an 8 deep 8-bit FIFO when operating in keyboard or strobed input modes. Each new valid entry is pushed into the FIFO and subsequently read in the same order in which it was pushed. The FIFO/RAM operates as an 8 Byte RAM when operating in scanned sensor matrix mode. As the sensor matrix is scanned, the inverted value of the return lines, RL[7:0], is written into the RAM address specified by the scan counter. In this way, the RAM maintains an image of the sensor array.

FIFO/RAM Status and Clear Control

The FIFO status logic keeps track of whether the FIFO is full or empty, and tracks the number of characters in the FIFO. In addition, an interrupt request signal, IRQ, is provided to signal the host microprocessor that the FIFO/RAM needs service. An overflow condition (attempting to push new data into a full FIFO) or underflow condition (attempting to read an empty FIFO) will be flagged as errors. The FIFO status can be read through the microprocessor interface when A0 is high. In FIFO mode, the IRQ output is asserted (high) when the FIFO is not empty. It is deasserted each time the FIFO is read, and is reasserted if unread data remains in the FIFO. In scanned sensor matrix mode, IRQ is asserted when the RAM contents are changed and is deasserted by writing to the EOI/Error Mode Set register. While IRQ is asserted, new writes to the RAM are inhibited.

Core Modifications

The XF8279 is designed to meet or exceed the AC Specifications of the industry standard 8279. However, in most cases the timespecs can be tightened significantly. In all cases, a post route timing analysis should be performed to verify performance. Implementation and customization are available through Memec Design Services.

Pinout

The XF8279 may be implemented internally with the user's design or as stand alone logic. For a fast replacement of the industry standard 8279, we provide a 40-pin device carrier which is pin compatible. Signal names are provided in the block diagram shown in Figure 1 and Table 1.

Core Assumptions

There is an important deviation in the design implementation. The internal timing is fixed to 8 MHz (using OSC4) and only the scan frequency is controlled by the external clock. The scan frequency is then synchronized with the internal clock. The reason for this is to meet and exceed the read and write cycle time. However, to our best understanding and practical experience, there are no deviations from the 8279 functional specifications.

Verification Methods

Basic functional simulation has been performed on the XF8279 using ViewSim. (Simulation vectors used for verification are provided with the core). VHDL and Verilog test benches are also provided. The design was also physically tested in three different environments and two different Xilinx FPGA devices without any problem.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
DB[7:0]	Input	**Input Data Bus**: Host microprocessor writes to core's control registers and Display RAM on this bus.
O_EN	Output	**Output Enable**: Asserted (low) when RD_L and CS_L are both asserted.
DBO[7:0]	Output	**Output Data Bus**: Host microprocessor reads core's RAMs and FIFO Status Word from bus.
RD_L_N	Input	**Read Strobe Net**: When asserted (low), the data source selected by a preceding control register write is placed on output data bus, DBO[7:0].
RD_L	Input	**Read Strobe**: A low to high transition terminates a read cycle.
WR_L	Input	**Write Strobe**: A low to high transition writes data from the input data bus, DB[7:0], into the XF8279's control registers or Display RAM.
CS_L	Input	**Chip Select**: Qualifies all host microprocessor read and write cycles; active low.
A0	Input	**Address Select**: Host microprocessor uses this signal to select whether current bus cycle is for data (A0 = 0) or for control registers and status (A0 = 1).
RESET	Input	**Reset**: High signal on this pin resets XF8279, after which it is placed in the following mode: 16 Character Display, Left Entry Keyboard Scan (Encoded) with 2-Key Lockout Prescaler Divisor set to 31.
RL[7:0]	Input	**Return Lines**:Inputs to XF8279 core from keyboard or sensor matrix. They also provide an 8-bit input in Strobed Input mode.
SHIFT	Input	**Shift**: In Scanned Keyboard modes, logic level of this input is stored with key position upon a valid key closure.
CNTL	Input	**Control/ Input Strobe**: In Scanned Keyboard modes, logic level of this input is stored with key position upon a valid key closure. In Strobed Input mode, it serves as the strobe line that enters the data into the FIFO on its rising edge.
GCLK	Input	**Internal Clock**: Processing clock to which all internal timing is synchronized. Industry standard 8279 used different counter chains, requiring many clock buffers. XF8279 has the bulk of its logic synchronized to this master clock.
CLOCK	Input	**System Clock**: Clock reference used to set scan frequency.
A[3:0] B[3:0]	Output	**Display Outputs**: May be treated as two 4-bit ports or one 8-bit port. Contents of Display RAM are presented on these outputs one Byte at a time, synchronized to the scan lines, SL[3:0], for multiplexed digit displays. The two 4-bit ports can be blanked independently.
IRQ	Output	**Interrupt Request**: In keyboard modes, IRQ is asserted (high) when data is in FIFO/RAM. IRQ is deasserted with each read of the FIFO/RAM and returns high if unread data remains. In sensor mode, IRQ is asserted whenever a sensor change is detected.
BD_L	Output	**Blank Display**: Asserted (low) during digit switching.
SL[3:0]	Output	**Scan Lines**: Used to scan keyboard or sensor matrix and display digits; these lines can be either encoded (binary counter) or decoded (1 of 4).

Recommended Design Experience

For the source version, users should be familiar with View-Logic Workview Office schematic entry and Xilinx design flows. For the netlist version, users should be familiar with Workview office, Xilinx Foundation, Verilog simulation/synthesis or VHDL simulation/synthesis. Users should also have experience with microprocessor systems.

Available Support Products

Memec Design Services supplies a Xilinx-based FPGA Development Module that can be used to hardware test this and other MDS cores. To purchase or obtain more information on XF8279 Programmable Keyboard Display Interface, contact Memec Design Services directly.

Ordering Information

The XF8279 Programmable Keyboard Display Interface is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

Information furnished by Memec Design Services is believed to be accurate and reliable. Memec Design Services reserves the right to change specifications detailed in this data sheet at any time without notice, in order to improve reliability, function or design, and assumes no responsibility for any errors within this document. Memec Design Services does not make any commitment to update this information.

Memec Design Services assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction, if such be made, nor does the Company assume responsibility for the functioning of undescribed features or parameters.

Memec Design Services will not assume any liability for the accuracy or correctness of any support or assistance provided to a user.

Memec Design Services does not represent that products described herein are free from patent infringement or from any other third-party right. No license is granted by implication or otherwise under any patent or patent rights of Memec Design Services.

Memec Design Services products are not intended for use in life support appliances, devices, or systems. Use of a Memec Design Services product in such application without the written consent of the appropriate Memec Design Services officer is prohibited.

All trademarks, registered trademarks, or servicemarks are property of their respective owners.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products
/logicore/alliance/tblpart.htm