

High Efficiency Microwave Power Amplifier: From the Lab to Industry

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Abstract

Since the beginnings of space travel, various microwave power amplifier designs have been employed. These included Class-A, -B, and -C bias arrangements. However, shared limitation of these topologies is the inherent high total consumption of input power associated with the generation of RF/microwave power. The power amplifier has always been the largest drain for the limited available power on the spacecraft. Typically, the conversion efficiency of a microwave power amplifier is 10 to 20 percent. For a typical microwave power amplifier of 20 watts, input DC power of at least 100 watts is required. Such a large demand for input power suggests that a better method of RF/Microwave power generation is required. The price paid for using a linear amplifier where high linearity is unnecessary includes: Higher initial and operating costs, Lower DC-to-RF conversion efficiency, High power consumption, Higher power dissipation and the accompanying need for higher capacity heat removal means, and an amplifier that is more prone to parasitic oscillation. The first use of a higher efficiency mode of power generation was described by Baxandall in 1959. This higher efficiency mode, Class-D, is achieved through distinct switching techniques to reduce the power losses associated with switching, conduction, and gate drive losses of a given transistor.

Purpose of the Paper

The purpose of this paper is twofold. First, to incorporate existing Class-D technologies used exclusively in the VLF-HF regime into microwave applications by combining current VLF-HF switching methodologies with innovative techniques to increase the overall DC-to-RF conversion of typical microwave power amplifiers.

Second, to develop new techniques for design of Class-D amplifiers to operate at microwave frequencies of several GHz. This is accomplished by proper generation and transmission of a microwave square wave throughout the power amplifier subsystem. This square wave case study presented here is new to power amplifier subsystems. Two patent application submissions have resulted from this research.

Significance of Study

There are important practical motivations for extending Class-D power amplifiers to the microwave regime. Severe technological constraints have made this goal elusive. This research has enabled new methodologies of microwave power amplification to be demonstrated, including a new type microwave power splitter/combiner, used exclusively for microwave Class-D power amplifier topologies. This new power splitter/combiner topology uses phasing techniques to allow propagation of square wave signals through a band-limited circuit.

By incorporating a High-Efficiency Microwave Power Amplifier (HEMPA) into a TDRSS standard transponder design, larger and more functional payloads can be supported even with the limited DC power.

Summary

In this paper, innovative and unique methods are developed and known to overcome limitations of current state-of-the-art microwave Class-D power amplifiers. These methods include creation of new types of microwave power splitter/combiner that are capable of propagating a microwave frequency square wave. This unique subsystem was designed and developed using current LF-HF topologies as a model with significant modifications to allow the accurate transmission of the microwave square wave.

With new results from this research incorporated into a Class-D microwave power amplifier an improvement of more than 50 percent in efficiency over traditional classes of operation is achieved. This improvement is enough to have a large favorable impact on any system with limited DC power.

History of the Class-D Amplifier

The Class-D amplifier concept has been in existence since the early 1960s. Baxandall was the first to designate the Class-D terminology while working with transistor sine wave generators from switching mode oscillators [2]. The Class-D (or High-Efficiency) amplifier has several distinguishing characteristics [3], [4]:

- High voltage across the device and large current through the device, though not at the same time,
- One or more transistors operating as single-pole switches, and
- Frequency of the output signal is the fundamental switching frequency.

Many applications in the Low-Frequency (LF) to High-Frequency (HF) amplifiers have used the Class-D amplifier extensively. Current state-of-the-art Class-D LF to HF amplifiers can achieve a DC-to-RF efficiency of 80-95 percent, and the literature contains similar results [5].

Currently NASA is using a second-generation transponder system that interfaces directly with the Tracking/Data Satellite System (TDRSS). This second-generation transponder, manufactured by Motorola Inc., is the backbone of the satellite to TDRSS link. This transponder is comprised of two main systems: the uplink and downlink telemetry systems. The downlink system operates in the 2200-2300 MHz region

with the uplink system operating in the 2100-2200 MHz region.

In the past, many hours were spent in the 'what-if' method of designing a new microwave power amplifier. Today, using high-speed computers these 'what-if' possibilities can be investigated in a much more expeditious and systematic method with accurate and reliable results.

The models from previous research have been used in simulations of the high-efficiency power amplifier topology. This simulation package [6], jOmega, is an RF/microwave general-purpose circuit simulation program developed by HP/EESof for nonlinear dc, nonlinear transient and linear ac analyses. Of particular interest is a new type of analysis exploring the harmonic-balance technique previously discussed.

The harmonic-balance method is iterative in nature, and is based on the assumption that for a given sinusoidal excitation there exists a steady state solution that can be approximated to satisfactory accuracy using a finite Fourier series. With the solution postulated in the form of a finite Fourier series, the circuit node voltages take on a set of amplitudes and phases for all frequency components. The currents flowing from nodes into linear elements, including all distributed elements, are calculated by a straightforward frequency domain linear analysis. Currents from nodes into nonlinear elements are calculated in the time-domain. Generalized Fourier analysis is used to transform from the time-domain to the frequency-domain [7].

Experimental Stage Analysis

The experimental stage is comprised of two NEC-9004-15 GaAs FETs biased in a Class-D arrangement and amplifies the transponder Receiver/Exciter (R/E) signal. This R/E signal can vary anywhere from +0 to +20 dBm (+10dBm nominal) into a 50Ω load. Reasons for the Class-D biasing arrangement included higher efficiency and maximum gain to generate as little additive noise as possible. The motivating force for the Class-D arrangement is the high-efficiency requirement.

After numerous simulations to arrive at the optimum performance, the following values were found. The overall RF gain from the stage was 15.4 dB with an input VSWR of 1.0024:1. The DC-to-RF conversion, also known as η , was 67.2 percent and the Power Added Efficiency (PAE)

is 65.2 percent. The PAE is defined as the RF output power minus the RF input power divided by the DC input power.

The final breadboard layout is shown in Figure 1.

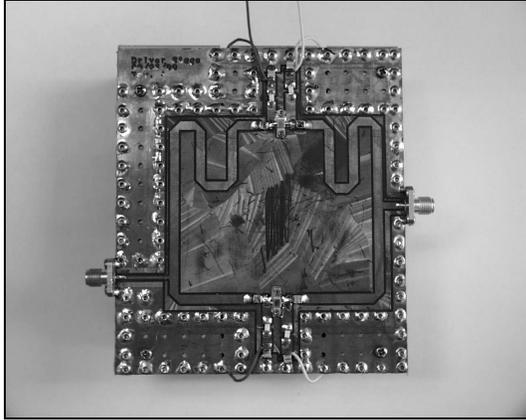


Figure 1—Final Breadboard Layout.

The actual breadboard layout was produced using the jOmega layout design tool. For this paper, the experimental stage was fabricated using a T-Tech milling machine. The fully populated board is approximately four inches square.

The test equipment included a RF signal generator, RF amplifier, DC power supplies for the gate and drain biasing, RF power meter, 30 dB attenuator, and band-pass filter.

The RF power meter, a Hewlett-Packard model 437B Power Meter, was used to measure the overall RF power spectrum, hence the need for the band-pass filter. The band-pass filter removed the harmonics from calculation of the power gain of the stage. The band-pass filter had a bandwidth of 2200-2300 MHz passing the 2250 MHz fundamental frequency.

The 30 dB attenuator was used to isolate the amplifier stage from the band-pass filter mismatch. In a Class-D amplifier, the harmonics as well as the fundamental must be terminated into 50Ω to achieve maximum efficiency. The 30 dB attenuator and band-pass filter was substituted for a properly designed diplexer.

The experimental stage has two NEC-9004-15 GaAs FETs biased in a Class-D arrangement, and amplifies the transponder receiver/exciter (R/E) signal. The input signal

can vary anywhere from +10 to +30 dBm (+20 dBm nominal) into a 50Ω load.

The first validation experiment was to vary the V_{dd} and V_{gg} voltages to find the optimum biasing arrangement for maximum efficiency with maximum gain. V_{gg} was varied from -2.5 to -1.0 VDC in 0.1 VDC increments and V_{dd} from 2.5 to 4.5 VDC in 0.25 VDC increments.

The first measurement dealt with VSWR, since the overall gain and efficiency of the stage (the true input power, which is dependent on VSWR) must be known, and this requires correction for VSWR.

The next measurement required the gain of the amplifier relative to the fundamental frequency (2250 MHz) with input power of +10 dBm. The first measured gain is relative to the total RF power (fundamental frequency only).

Using (1) and (2) along with the forward and reflected power, given in milliwatts, ρ is determined.

$$P_r = P_i \rho \quad (1)$$

Where P_i is the incident power (in this case +10 dBm) and ρ is the reflection coefficient given by

$$\rho = \frac{(VSWR - 1)}{(VSWR + 1)} \quad (2)$$

The actual output power, from the gain and VSWR-corrected power is then determined.

Using the values determined above and (3) the efficiency vs. V_{dd}/V_{gg} is determined.

$$\eta = \frac{P_{out}}{P_{DC} + (P_{in} - P_{ref})} \quad (3)$$

The results show that the maximum and minimum values for the efficiency are 51.9 percent and 36.2 percent, which corresponds to $V_{dd} = 2.50$ VDC, $V_{gg} = -2.3$ VDC, and $V_{dd} = 4.50$ VDC, $V_{gg} = -3.0$ VDC, respectively.

This configuration allowed the greatest efficiency but not the highest gain, which have the respective behavior shown in Figure 2. The optimum bias configuration is such that the amplifier exhibits the highest gain with the highest efficiency.

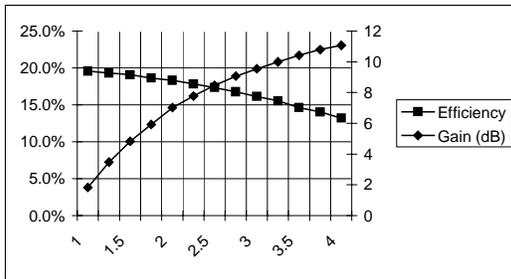


Figure 2—Comparison of gain and efficiency – Experimental stage.

Because the gain of the amplifier is a function of V_{dd} , V_{gg} , and I_{dd} and the efficiency is a function of the same parameters, the following can be accomplished. Taking the product of the efficiency and Gain vs. V_{dd}/V_{gg} would generate a maximum gain-efficiency plot and is shown in Figure 3.

The result is for an approximate 5 percent decrease in the maximum efficiency (where $V_{dd} = 2.5$ VDC and $V_{gg} = -3.0$ VDC) an increase of 3.0 dB in gain (where $V_{dd} = 3.75$ VDC, and $V_{gg} = -2.0$ VDC) can be achieved.

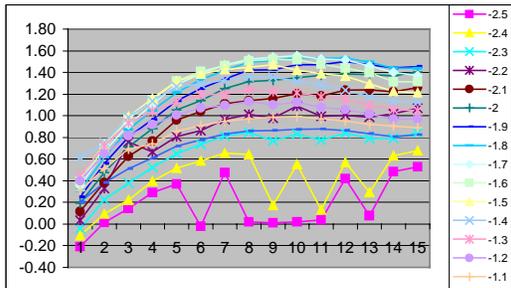


Figure 3—Gain - Efficiency product.

Consequently, the final amplifier exhibits 9.1 dB of gain with an efficiency of 40.2 percent - which is almost twice the efficiency of a typical S-band amplifier. If the efficiency is considered more important than the gain then maximum efficiency could be biased for an efficiency of 49.5 percent, but with a gain of 6.72 dB

Summary

The actual breadboard layout was produced using the jOmega layout design tool.

A systematic measurement program validated the computer simulations. Tests included input VSWR, input DC power, and output RF power. From these measurements, the overall operation of the experimental stage was found to agree favorably with the computer

simulations. The overall final efficiency of the experimental stage was 49.5 percent, almost five times better than a typical commercially available S-band amplifier today.

Recommendations

Overall, for a new design of a high-efficiency microwave power amplifier, the outcomes were positive. In this paper, it is shown that at a minimum the overall efficiency of a typical microwave amplifier can be improved to approximately 50 percent. To further exploit these results, three recommendations for future work are offered.

The first recommendation is the need to increase the fidelity of the power device models. The IC-CAP software is helpful in extracting and generating the individual transistor parameters. However, since no system is completely accurate, better transistor models should be pursued. Because simulations are only as good as the models that are used, it makes little sense to invest large amounts of time and money in a simulation only to find that the models were inaccurate. During this research, hundreds of iterations were required to generate a usable transistor model.

The second recommendation is to improve on the ability of jOmega to accurately complete a simulation. Special techniques had to be incorporated into the simulation-input file to generate meaningful simulations. Convergence errors needed special attention, arising from two unrelated simulation requirements. The first requirement is high-power level simulations. As the power levels involved with the circuit are increased, there is a threshold where jOmega becomes unstable (most noticeable in the high power regime). Special input file inclusions alleviated some of these problems, but each time a circuit parameter is changed, the technique has to be changed to allow a successful simulation.

The second simulation requirement is the need for bias-dependent models used. Currently jOmega can only do non-linear simulations on bias-dependent devices. This is a severe limitation when trying to simulate Class-D amplifiers, where the device is in either cut-off or saturation. Some form of multiple bias levels in the model must be undertaken.

The third recommendation is for more work on the advancement of wider bandwidth power devices. Currently, the devices being used have a unity gain at approximately 18 GHz. As this is increased through future revisions to the actual power devices, more efficient power

amplifiers can be achieved. As the technology improves, so will the Class-D amplifier.

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