# SRM Inverter Topologies: A Comparative Evaluation

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*Abstract*—**Several inverter power circuits that are suitable for switched reluctance motor (SRM) drives are analyzed and compared with each other. The comparison is based on the peak voltage and current ratings of the power switches and on the size and peak ratings of the dc-link components. Because the converter choice depends on the motor design, the converter analysis and selection are done for a high-speed, 6/2 SRM suitable-for-a-spindle drive and a high-torque 8/6 motor. Experimental results obtained for a high-torque drive are included.**

## I. Introduction

Although SRM drives have not yet found broad industry acceptance, they continue to attract research interest, stimulated mainly by the promise of simple and rugged motor construction, the possibility of high motor speeds, high torque-to-inertia ratio, an inverter with a reduced number of power switches, and an overall robust drive. This research activity has resulted in a number of inverter topologies, some of which have been described in the literature [1]–[6]. However, although a comparison of the required kVA ratings between an SRM and an induction drive inverter was done [7], no comparison exists between different inverter topologies that are suitable for an industrial SRM drive.

This paper considers five inverter circuits, represented in Fig. 1 with the objective of establishing the most appropriate topology for an SRM drive. Although there are other inverter circuits that could be considered for this application, the five circuits analyzed here are possibly the most promising. Some of the circuits that have not been considered as appropriate are, for example, the circuit described in [4], which is restricted to very low speed motors by providing essentially constant dc-link current; the circuit given in [5], which, among other disadvantages, does not have an inherent protection against a shoot-through; the circuit presented in [6], which provides a minimum number of active switches for an 8/6 motor but cannot provide sufficient demagnetization voltage in the presence of the current overlaps encountered in 8/6 motors, etc. Not considered in this paper is another class of inverter topologies for motors with bifilar windings.

As the study progressed, it became evident that the suitability of a particular inverter circuit changes with the motor

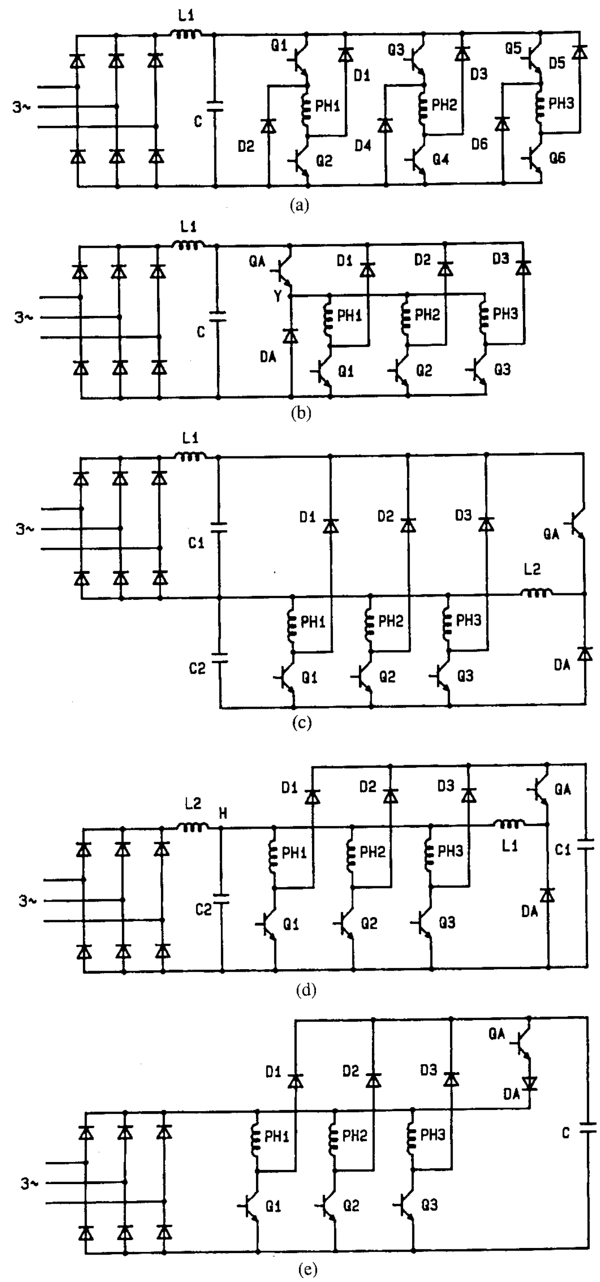


Fig. 1. The five circuits analyzed in this study: (a) No. 1; "classic" inverter; (b) no. 2, Miller circuit; (c) no. 3, buck-boost inverter; (d) no. 4, C-dump inverter; (e) no. 5, sood inverter.

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geometry, making an absolute, general choice impossible. Note that this is in contrast to drives operating with sinusoidal voltages or currents where the inverter topology is independent of the motor design. Specifically, in the case of SRM's, it was found that the number of the stator/rotor poles and the related issues of the dwell angle and current overlap (current being injected into one phase, while the adjacent phase current is still flowing) affect the inverter choice. For that reason, the study was expanded to include a high-speed 6/2 motor, presented in Fig. 2 and a high-torque 8/6 motor, shown in Fig. 3. These two drives are then examined separately and the most suitable inverter circuit for each one is identified. As will be seen, the key parameter affecting the inverter selection is whether a motor operates with or without an overlapping current through its speed range. Thus, although it is based on two motor geometries, the analysis presented in this paper can be generalized to all SRM's by using current overlapping as the dividing criterion.

In Section II, principles of a motor operation are briefly examined in order to define the requirements for a SRM inverter. Following that, the operation of each inverter circuit, presented in Fig. 1 is described, the equations for a selection of circuit components are identified, the inverter total kVA rating is determined, and the inverter suitability is evaluated against the requirements defined by motor operation.

After that, the power components of the five inverters (Fig. 1) are chosen for a 10-kW drive, first for the 6/2 and then for the 8/6 motor. The most suitable inverter circuit is then selected, primarily by considering the total required VA inverter rating. Finally, experimental results, obtained with the 8/6 drive and the inverter circuits from Fig. 1 are presented.

## II. Basic Motor Requirements

The material given in this section is available in the literature and is included here only for the sake of completeness and in order to define the required inverter characteristics.

Unlike in machines with distributed windings, the energy conversion in SRM's occurs in discrete cycles (sometimes called strokes), through the interaction of one stator and one rotor pole pair. Fig. 4 shows a typical change in the stator self-inductance as a function of rotor position, while Fig. 5 defines the corresponding angles. The flat portion of the $L_{\max}$ curve (dead zone, [1]), Fig. 4, is caused by a difference in the width between the stator and rotor poles. This flat portion is normally provided to avoid or reduce negative torques during demagnetization. Usually the stator poles are made more narrow, thus providing more space for the windings at the same time.

The winding is normally connected to a voltage source prior to the angle $\Theta 1$, giving rise to a stator current, Fig. 6. The current waveform depends on the motor speed, the forcing voltage, the winding total inductance, and the turn-on angle $\Theta$s. If the polarity of the voltage connected across the motor phase is reversed at $\Theta = \Theta 2$, a demagnetization begins. The waveform of the resulting current tail, $\Theta 2 - \Theta E$ depends on the forcing voltage, the stored magnetic energy, and the motor speed. If the current flows beyond $\Theta = \Theta 3$, a negative torque is generated, Fig. 6. The current and torque waveforms, Fig. 6 are qualitative only and will vary with the motor operating conditions and the motor geometry.

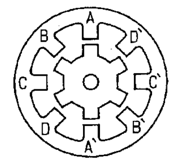


Fig. 2. High-speed 6/2 SRM.

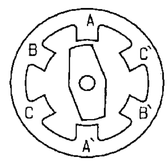


Fig. 3. High-torque 8/6 SRM.

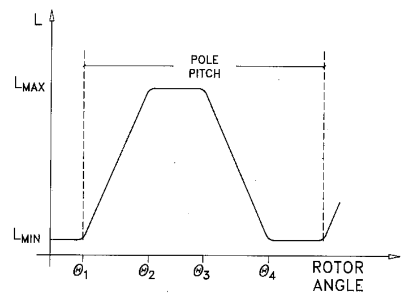


Fig. 4. Variation of stator phase inductance with rotor position.

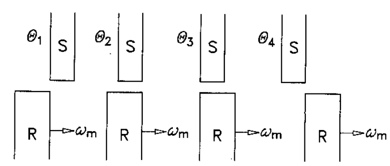


Fig. 5. Definition of rotor angles.

Due to requirements for high starting torques, and/or reduced torque ripple, the energy conversion process may occur simultaneously in two adjacent phases, causing a current overlap (Fig. 7). As will be seen later, the existence of the overlap at high motor speeds eliminates some inverter circuits from consideration. It is obvious from Fig. 4 that the motor torque can be increased by widening the range $\Theta 1 - \Theta 2$, where the inductance change $dL/d\Theta$ has a positive slope. Because this range is proportional to the width of a stator pole, one would design a motor with wide stator poles. On the other hand, wide poles lead to a current overlap whereas at the same time, due to increased inductance, limit the motor maximum speed for a given supply voltage.

It is instructive to establish the limit conditions for a current overlap. Denote by $N_s$ and $N_r$ the number of stator

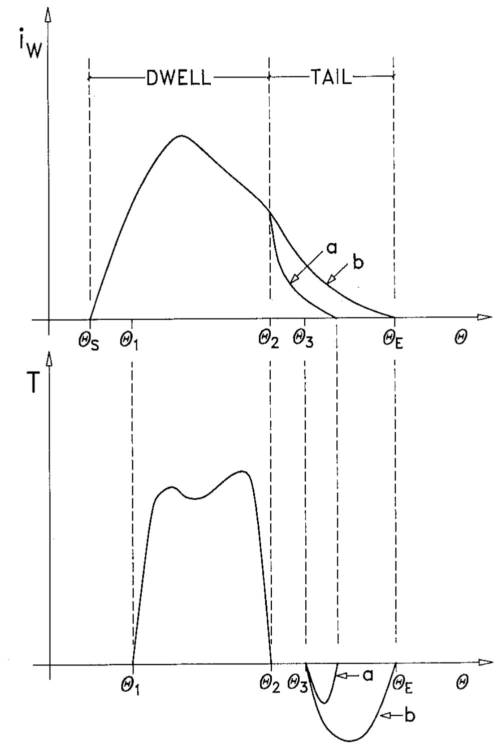


Fig. 6. Qualitative representation of current and torque during one energy cycle. Negative torque is produced when current flows past $\Theta = \Theta 3$.

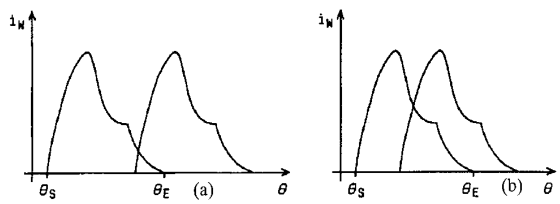


Fig. 7. Definition of the current overlaps: (a) Tail; (b) dwell.

and rotor poles, respectively, by $N$ the number of phases, by $PW$ the width of the stator pole, and by $K_1$ the ratio of a stator pole width and a pole pitch. Assuming that the rotor poles are wider or equal to the stator poles, the stator pole width is

$$PW = 360 \times K_1 / N_s.$$

The pole width $PW$ is equal to the arc over which $dL/d\Theta$ is positive. Denote by $K_2$ the ratio between the width of the current pulse, $CW = \Theta s - \Theta E$ (Fig. 6) and the width of the arc over which $dL/d\Theta$ is positive so that

$$CW = (K2) \times (PW). \tag{1}$$

On the other hand, the number of current pulses per one turn is $N \times N_r$. The width of this pulse is $360/(N \times N_r)$. Obviously, then, the limit of a current overlap exists if

$$360/(N \times N_r) \geq 360 \times K_1 \times K_2 / N_s$$

from which it follows that the limiting width of the current pulse is

$$K_2 \leq N_s / (N \times N_r \times K_1). \tag{2}$$

As an example, assume that the stator pole occupies half of the pole pitch $K_1 = 0.5$. For an 8/6 geometry, (2) gives $K_2 \leq \frac{2}{3}$, which is impractical. (To avoid the overlap, the current should flow only during approximately two thirds of the interval when $dL/d\Theta$ is positive (1)). For a 6/4 motor, the result is $K_2 \leq 1$, which is also impractical. The 6/2 motor gives $K_2 \leq 2$, which is realistic and acceptable, after the motor has started.

This discussion indicates that most SRM's operate with a current overlap. One needs then to do a detailed verification to determine if a given inverter circuit can provide the necessary voltages in the speed range when a current overlap exists. Consider briefly now the issue of the motor constant power range. As the motor speed is increased, the time available for winding magnetization $t_m$ decreases:

$$t_m = \frac{\text{dwell}}{\omega}. \tag{3}$$

If $V$ is the magnetizing voltage, the flux per pole is proportional to

$$\Phi \sim t_m \times V = \text{dwell} \times \frac{V}{\omega}.$$

Since SRM's are single excited machines, the torque is proportional to

$$T \sim \Phi^2 \sim \left(\text{dwell} \times \frac{V}{\omega}\right)^2 \tag{4}$$

while the motor power is

$$P = T \times \omega \sim \frac{(\text{dwell} \times V)^2}{\omega} \tag{5}$$

From (4) and (5) it is clear that SRM's are not well suited for operation over a wide speed range above the rated speed. The situation is improved by using a motor with low-speed windings, having a large number of turns, and, in the other phase, a high-speed winding with a small number of turns. Although such a motor will have a somewhat higher current at starting in the high-speed winding, its speed range would be considerably increased. Such an approach is used on the 6/2 motor (Fig. 2) which is further described in Section IV [8].

From this discussion one can formulate some functional requirements that an SRM inverter should ideally meet:

1) It needs to control the voltage applied to the winding at low speed, so as to limit the winding current. Either voltage or current PWM control can be used.
2) It needs to have sufficiently high forcing voltage, at each operation point so that the current is injected sufficiently quickly into the winding (Fig. 6). Obviously, this requirement is critical at high speeds since the time available is decreased, $t = \text{dwell}/\omega$.
3) It has to have as high a demagnetizing voltage as

possible in order to shorten the current tail, thus avoiding negative torques and/or permitting an extension of the dwell angle (Fig. 6).

4) It has to provide independent control of phase currents in motors having current overlap (Fig. 7) so that energy can be supplied to one phase while extracting it simultaneously from the other phase.
5) It has to provide efficient energy recycling during a demagnetizing interval. This is an important requirement given the highly cyclical energy exchange between the inverter and the motor.
6) It should isolate the ac network from the current pulse shocks caused by the motor. On the other hand, with a three-phase ac supply, the motor is practically insensitive to the rectifier output ripple.

Finally, one should note that the inverter current rating is determined by the starting torque requirements, whereas the voltage rating is fixed by the maximum motor speed. Specifically, in the next section, current overlap is assumed at starting and each inverter circuit is dimensioned accordingly. In order to arrive at an economically acceptable design procedure, the starting current per phase is limited to the rated winding current, defined by the motor rated torque. In the case of SRM's, this generally yields starting torques lower than the rated torque, depending on the rotor initial position.

## III. Inverter Circuits

Before the five circuits (Fig. 1) are discussed, it is useful to divide all SRM inverters into two groups: single-rail inverters and dual-rail inverters. The single-rail circuit is characterized by having the same voltage available for the magnetizing and demagnetizing of the motor phases. In the dual-rail circuit, two voltages are used. In Fig. 1, (a) and (b) show the single-rail inverters, whereas (c), (d), and (e) are the dual-rail inverters.

Each inverter is now described and the procedure to calculate the circuit elements is presented. In order to avoid confusion, the calculations and the numerical values in Sections IV and V do not include the normal design margins, nor do they include the rounding of the calculated values to the nearest available component value. The following notation is used to calculate inverter components:

| | |
|---|---|
| $N$ | number of motor phases |
| $N_s$ | number of stator poles |
| $N_r$ | number of rotor poles |
| $\omega_n$ | base (rated) motor speed, rad/s |
| CEMF | motor counter electromotive force, V |
| $V$ | input ac line-to-line rms voltage, V |
| $V_{dc}$ | rectified dc voltage, $V_{dc} = 3V\sqrt{2}/\pi$, V |
| $DV$ | relative increase of the capacitor voltage |
| $I_{pw}$ | peak value of the phase winding current, A |
| $I_{rmsw}$ | rms value of each phase current, A |
| $W_t$ | total energy a winding receives during a dwell period |
| $X$ | percentage of $W_t$ returned to inverter, $0 < X < 1$ |
| $W_r$ | energy returned to inverter during demagnetization |

$$W_r = X \times W_t \tag{6a}$$

| | |
|---|---|
| $P$ | average power supplied to the motor during dwell angle, W |
| $P_n$ | motor active input power, W |

$$P_n = P \times (1 - X) \tag{6b}$$

### A. Calculating the Input Rectifier and the dc Link Filter

In selecting the dc-link choke to obtain a limit of continuous conduction at a rated load, the rectifier peak current $I_p$ and the choke dc current $I_{dc}$ are

$$I_p = 2 \times I_{dc} = \frac{2 \times P_n}{V_{dc}} \tag{7}$$

while the choke rms current is $I_{rms1} = 1.227 I_{dc}$. The rms current of the dc-link capacitor and the minimum capacitor values are, respectively,

$$I_{rmsC} = \sqrt{(I_{rmsL})^2 + N \times (I_{rmsw})^2 - 2 \times (I_{dc})^2} \tag{8}$$

$$C_{min} = W_r/(DV \times V_{dc}^2) \tag{9}$$

where $W_r$ is the average energy returned to the inverter during each stroke

$$W_r = \frac{A}{B} \tag{10a}$$

$$A = X \times P \qquad B = N \times N_r \times \omega n/(2\pi) \tag{10b}$$

where $A$ is the average power returned to the inverter by all phases and $B$ is the total stroke frequency.

### B. Circuit 1: Classic Inverter

The classic inverter (Fig. 1(a)) is a well-known single-rail circuit, requiring $2N$ active switches. The motor phases are controlled independently of each other. Each inverter leg/motor phase has three possible states. Considering phase 1, they are:

State 1: Magnetization. Both Q1 and Q2 are on.

State 2: Freewheeling. The winding is short circuited either through Q1 or Q2 and the rate of demagnetization is low.

State 3: Forced demagnetization. Both Q1 and Q2 are off. The winding current charges the capacitor $C$ against the dc-link voltage.

During low-speed operation, the available voltage exceeds by far the motor CEMF, and the magnetizing current has to be PWM controlled by alternating between states 1 and 2. The energy-conversion cycle is completed by switching to state 3. As the motor CEMF increases with the speed, the available time becomes shorter, whereas the voltage requirements increase and the operation is transferred to a single-pulse mode (Fig. 6). The inverter design follows.

The peak voltage rating, transistor $Q$, and diodes $D$ (Fig. 1(a)) are

$$V_pQ = V_pD = V\sqrt{2}(1 + DV). \quad (11)$$

The transistor peak current, $I_pQ$, is defined by the motor starting requirement. Note that the current overlap does not affect switch rating since each phase operates independently. The diode current rating is determined by the braking requirements and is selected here to be equal to that of the transistors.

Thus, the device rating is:

| | |
|---|---|
| Voltage rating, all devices | $V\sqrt{2}(1 + DV)$ |
| Current rating, all devices | $I_{pw}$ |
| Total active devices, kVA | $2N \times I_{pw} \times V\sqrt{2}(1 + DV)$ |

The current rms and peak values can be determined only if the motor design and control angles are known.

The main advantages of the "classic" converter, (Fig. 1(a)) are the independent control of each of the motor phases and the relatively low voltage rating of the inverter components. The main disadvantages are the total number of switches, the dc link filter, and a relatively low demagnetizing voltage at high speeds.

### C. Circuit 2: Miller's Inverter

This single-rail inverter circuit has been reported by T. Miller *et al.* [9] and is shown in Fig. 1(b). This circuit is derived from the "classic" inverter by substituting switches Q1, Q3 and Q5 by QA and diodes D2, D4, and D6 by DA. In this way, the number of switches as well as the number of motor leads is reduced to $N + 1$. The circuit has three operating states, which are analogous to those in the "classic" inverter. Considering phase 1:

State 1: Magnetization. Both QA and Q1 are on.
State 2: Freewheeling. Q1 is on, QA is off, and the current freewheels through Q1 and DA. The flux changes slowly, depending on speed.
State 3: Forced demagnetization. Both QA and Q1 are off. D1 and DA conduct and the magnetic energy is transferred to the capacitor $C$. The demagnetization proceeds quickly against the dc link voltage.

The main limitation of this inverter is that with QA on, a forced demagnetization of any of the phases is not possible. Consider first operation at low speed, with a PWM control of the winding voltage. In order to provide at least some demagnetizing voltage to another phase, Q1 is on while QA is PWM controlled. If the duty cycle is sufficiently low, that is, if the average voltage $VY$ applied to the winding of phase 1 is sufficiently small, another phase can still be demagnetized with the voltage $V_{dc} - VY$. As the voltage required by the winding increases with the motor speed, the voltage at the $Y$ point is increased and the demagnetization voltage $V_{dc} - VY$ is decreased. Thus, when using this inverter circuit, one needs to calculate the limiting speed below which there is a sufficient demagnetization voltage, even with a tail overlap. Experience indicates that with high-speed SRM's having a relatively low inductance per pole, this value approximately corresponds to $VY = 0.5V_{dc}$.

The device ratings are essentially the same as for the "classic" inverter, except for the QA and DA currents, which are, under the worst-case condition of a dwell overlap during motor starting, approximately twice the phase-winding current.

| | |
|---|---|
| Voltage ratings, all devices | $V\sqrt{2}(1 + DV)$ |
| Current rating D1–DN and Q1–QN | $I_{pw}$ |
| Current rating QA and DA | $2I_{pw}$ |
| Total kVA, active devices | $(N + 2) \times I_{pw} \times V\sqrt{2}(1 + DV)$ |

As will be seen, this topology offers the lowest inverter kVA and is clearly advantageous providing the current overlap does not pose a problem.

### D. Circuit 3: Buck-Boost Inverter

To the best of our knowledge, this dual-rail circuit with $N + 1$ active switches (shown in Fig. 1(c)) has not been published before. The circuit offers an added flexibility in motor control by separating the magnetizing ($V_{c1}$) from the demagnetizing ($V_{c2}$) voltage. Considering phase 1 only, the inverter operation can be divided into four states:

State 1: Magnetization. Q1 is on, impressing the $V_{c2}$ voltage across the winding.
State 2: Forced demagnetization. Q1 is off. D1 conducts, transferring the winding magnetic energy to C1. The voltage across Q1 is $V_{c1} + V_{c2}$.
State 3: Discharging of C1. QA is on, discharging C1 while building the current in L2. Note that the ac line contributes to the L2 current.
State 4: Charging of C2. QA is off. DA conducts, transferring the energy stored in L2 to C2. The voltage across QA is $V_{c1} + V_{c2}$.

The following comments can be made with respect to the operation of the buck-boost inverter:

- Since all the identified states are noninteracting, each phase can be controlled independently and the current overlap is not a problem. Also, by operating independently of the motor phases, the boost chopper can control continuously the C1 and C2 voltages.
- PWM control of phase switches Q1–Q3 is not necessary if the C2 voltage is continuously regulated to satisfy the magnetization requirements at each speed. However, this means that the motor-starting currents, with dwell overlap, have to be entirely supplied through QA, requiring an increased QA rating. Since C2 is intentionally kept small, it is not practical to precharge C2 and to supply the starting currents partially from C2.
- If desired, it is possible to boost the C2 voltage significantly above the ac-rectified voltage $V_{c1}$ thereby increasing the motor maximum speed for a given ac line voltage. (However, for a given inverter power, the QA rating is minimum when $V_{c1} = V_{c2}$. Also, the current tails would be longer than the dwell period.)

• It is possible to reduce the ac line harmonics by eliminating L1, reducing C1, and using the boost chopper to waveshape the ac line currents. In this case, however, a degree of freedom is lost and a compromise needs to be made between regulating the C2 voltage and waveshaping the ac input currents.

The ratings of the inverter components are now determined, beginning with a chopper, which is dimensioned for the motor starting. Assume that the winding current is constant and equal to its peak value $I_{pw}$. Assume further that there is a dwell overlap at starting between the two phase currents so that the average current supplied by C2 is $2I_{pw}$. The same current has to be supplied by the diode DA as follows:

$$I_{dc}\mathrm{DA} = I_{dc}\mathrm{C2} = 2 \times I_{pw}. \tag{12a}$$

If the QA modulation index is $m$, then during the interval $m$ the DA current is zero, whereas during the $1 - m$ interval the DA current equals the L2 current:

$$I_{dc}\mathrm{DA} = (1 - m) \times I_{dc}\mathrm{L2}. \tag{12b}$$

Also, the peak QA current is

$$I_p\mathrm{QA} = I_{dc}\mathrm{L2}(1 + R) \tag{12c}$$

where $R$ accounts for the current ripple $\Delta I$ in L2:

$$\Delta I = R \times I_{dc}\mathrm{L2}.$$

From (12a), (12b), and (12c) the current rating of the chopper switch QA is

$$I_p\mathrm{QA} = 2 \times (1 + R) \times I_{pw}/(1 - m). \tag{13a}$$

The last expression can be simplified. Consider

$$m \times V_{c1} = (1 - m) \times V_{c2}.$$

Assuming that the $V_{c2}$ voltage at start up is regulated to be 3% of the $V_{c2}$ voltage, one obtains $m = 0.029$. Furthermore, assuming very conservatively that the current ripple in L2 is 5%, so that $R = 0.05$, the final rating for QA becomes

$$I_p\mathrm{QA} = 2 \times 1.08 \times I_{pw} = 2.16 \times I_{pw}. \tag{13b}$$

The rms current in the chopper inductance L2 is

$$I_{rms}\mathrm{L2} = I_{dc}\mathrm{L2}\sqrt{1 + \frac{R^2}{3}}. \tag{14}$$

The chopper inductance is

$$\mathrm{L2} = \frac{V_{dc}}{4 \times f_c \times R \times I_{dc}} \tag{15a}$$

where $f_c$ is the chopper's PWM frequency. Capacitor C1 should not be smaller than

$$\mathrm{C1(min)} = Wr/(DV \times V_{dc}^2) \tag{15b}$$

where the energy returned to the inverter during demagnetization $W_r$ is given by (10). However, the capacitor value will most likely be determined based on the rms current rating as follows:

$$I_{rms}\mathrm{C1} = \sqrt{I_a^2 + I_b^2 + I_c^2} \tag{16a}$$

where $I_a$ is the ac current component flowing through L1:

$$I_a^2 = (I_{rmsL1})^2 - (I_{dc})^2 \tag{16b}$$

while $I_b$ is the ac component flowing through QA and L2:

$$I_b^2 = \frac{(I_{rmsL2})^2}{2} - \left(\frac{I_{dcL2}}{2}\right)^2 = \left(\frac{P}{V_{dc}}\right)^2 \frac{1 + 2(R^2/3)}{4}. \tag{16c}$$

The ac component of all tail currents, denoted by $I_c$ and flowing through C1 during the demagnetization period, can be calculated once the motor characteristics and the control parameters are known. The capacitor C2 is also selected on the basis of the total ac current components:

$$I_{rmsC2} = \sqrt{I_b^2 + I_d^2} \tag{17}$$

where $I_b$ is the ac component of the diode DA current. Because DA is dimensioned for the rated motor speed (50% duty cycle), the $I_b$ current is equal to that of QA ((16c)). The $I_d$ current is the ac component of the winding currents.To calculate $I_d$, one has to know the waveform of the phase currents. One should check that the C2 value, calculated from (17), is not smaller than

$$\mathrm{C2(min)} = \frac{I_{dcL2}}{4 \times f_c \times V_{dc} \times DV} \tag{18}$$

where $DV$ is the allowed percentage voltage overshoot on C2. This overshoot is obviously determined by the dynamics of the voltage regulator, controlling QA. With a high chopping frequency, $f_c$ and a fast chopper regulator, both L2 and C2 can be relatively small. Assuming for the moment that voltage overshoots on C1 and C2 are equal, that is, $DV_{c1} = DV_{c2} = DV$, the component ratings of the buck-boost converter are as follows:

| | |
|---|---|
| Voltage rating for all devices | $2V\sqrt{2}(1 + DV)$ |
| Current rating for Q1–QN and D1–DN | $I_{pw}$ |
| Current rating for QA and DA | $2.16I_{pw}$ |
| Total kVA, active devices | $2 \times (N + 2.16) \times I_{pw} \times V \sqrt{2}(1 + DV)$ |

The main advantages of the buck-boost inverter are the flexibility in motor control, the ability to tailor the C2 voltage to the motor needs and thus avoid a PWM control of the phase switches, the noninteractive winding control, permitting current overlap, and the possibility of waveshaping of the input currents. The main disadvantage is the required double-voltage rating on all devices, the need to process the entire motor input power through the chopper, and the large number of passive components.

### *E. Circuit 4: C-Dump Inverter Circuit*

This circuit, shown in Fig. 1(d), has been described by Ehsani *et al.* [3]. It is a dual-rail circuit, transposed with respect to the buck-boost inverter: the motor phases are supplied form the rectified voltage stored on C2, whereas the magnetic energy, stored in C1, is transferred to C2 through the chopper consisting of QA, L1, and DA. A modified C-dump circuit is obtained by connecting the capacitor C1 between QA and point $H$ (Fig. 1(d)). Such modification would be desirable because the voltage available for demagnetization would be $V_{c1}$ instead of $V_{c1} - V_{c2}$ as in Fig. 1(d). (Or, with the same demagnetizing voltage, the voltage rating of C1 would be approximately halved.) However, this paper considers the original circuit as reported in [3]. The inverter has four possible operating states functionally identical to those in the buck-boost inverter. Considering phase 1:

State 1: Magnetization Q1 is on and C2 is connected across the winding, supplying the magnetizing current.
State 2: Forced demagnetization. Q1 is off and the demagnetizing current circulated through D1, C1 and C2. The rate of demagnetization is determined by the voltage difference $V_{c1} - V_{c2}$. The voltage across Q1 is $V_{c1}$.
State 3: Discharging of C1. QA is on and the current loop is closed through L1, C2, and C1. The C2 voltage increases as the current builds up through L1.
State 4: Completion of charging of C2. QA is off and the current circulates through L1, C2, and DA, transferring energy stored in L1 to C2. The voltage across QA is $V_{c1}$.

The C dump is very similar to the buck-boost inverter and the same comments, given in Section II, apply here. The only differences between these two circuits are that:

- Because the phases are supplied from the uncontrolled rectified voltage $V_{c2}$, each phase switch, Q1 − QN needs to perform PWM control at low speed. As a result, a large portion of the energy is transferred to C1 and, then again, through the chopper action, back to C2.
- The average C1 voltage is approximately twice the C2 voltage in order to have equal magnetizing and demagnetizing voltages.
- By turning on Q1 and QA simultaneously (operating concurrently in states 1 and 2) it is theoretically possible to increase the motor-supply voltage and thereby increase the maximum motor speed. This mode of operation is called synchronous chopper control [3]. In practice, however, insertion of L1 inductance into the motor magnetizing loop is contrary to the desire for a fast magnetization at high speed. Furthermore, C1 is discharged during the dwell period and becomes ill prepared for the demagnetization requirements of a short current tail.

For these reasons, the maximum winding magnetizing voltage is practically fixed by the ac lines. For the same reason as above, wave shaping of the ac input currents, and thus the ac line harmonic control, is not possible. Although the C-dump chopper has to process only the demagnetizing power XP instead of the full inverter power P in case of the buck-boost inverter, there is very little difference in their ratings as both choppers have to be dimensioned for the starting currents, which are approximately the same for the two circuits. The C-dump components can be selected using the same equations as for the buck-boost circuit, with these exceptions:

$$I_{\mathrm{dcL1}} = X \times \frac{P}{V_{\mathrm{dc}}} \tag{19}$$

where $P$ is the rated converter power $P = Pn/(1 - X)$ and XP is the demagnetizing power transferred from C1 to C2. Also, the expression for the minimum value of C2 has to be modified. With the C-dump circuit, the total energy stored in C1 is

$$W_r\mathrm{C1} = W_r + W_2 \tag{20}$$

where $W_r$ comes from the winding magnetic energy, (10a), and $W_2$ comes from the capacitor C2. If $V_{c1} = 2V_{c2}$, $W_r = W_2$ so that the energy stored on C1 is $2W_r$. This energy needs to be transferred through the chopper to C2, which then becomes

$$\mathrm{C2(min)} = 2W_r/\left(DV \times V_{\mathrm{dc}}^2\right) \tag{21}$$

or twice the value given by (15b) for the corresponding capacitor in the buck-boost inverter.

To size QA, consider the motor just starting Assume that switches Q1–QN are PWM controlled with a 50% duty cycle and that QA is also operating with a 50% duty cycle to give $V_{c1} = 2V_{c2}$. Furthermore, assume that each phase draws the peak current $I_{pw}$ and that there is a dwell overlap between the currents in two phases. Under these conditions, the average current charging C1 is $0.5I_{pw} + 0.5I_{pw}$ while the average current discharging C1 is $0.5I_{\mathrm{dc}}\mathrm{L2}$. Obviously, the charging and the discharging currents must be equal. Also, the peak QA current is

$$I_p\mathrm{QA} = I_{\mathrm{dc}}\mathrm{L2}(1 + R) = 2 \times I_{pw}(1 + R). \tag{22}$$

Assuming that the ripple in L2 is 5% ($R = 0.05$), the component ratings for the C-dump inverter become

| | |
|---|---|
| Voltage rating, all devices | $2 \times V\sqrt{2}(1 + DV)$ |
| Current rating, Q1–QN and D1–DN | $I_{pw}$ |
| Current rating, QA and DA | $2.1 \times I_{pw}$ |
| Total kVA, active devices | $2 \times (N + 2.1) \times \underline{I_{pw}} \times V$ $\sqrt{2}(1 + DV)$ |

### *F. Circuit 5: Sood's Inverter*

This circuit, presented in Fig. 1(e), is the last dual-rail topology considered. Because this is a new circuit [10], its operation is discussed in some detail. The main circuit characteristic is the elimination of a dc link inductance and a capacitor and the direct transfer of the capacitor energy to the motor windings. It is believed that this is the minimum component topology. Although this circuit is similar to the C-dump inverter (and thus also to a buck-boost configuration), its modes of operation are fundamentally different. Considering phase 1, one can identify four operating states:

State 1: Magnetization from the ac line. Q1 is on and the phase winding is connected to the unfiltered rectified voltage $V_r$.

State 2: Magnetization from the capacitor. Both Q1 and QA are on. With the capacitor voltage $V_c$ being larger than the rectified voltage $V_r$, the input rectifier is reverse biased and the energy flows from the capacitor to the winding. The supplied power is P2 = $(V_c)(I_w)$. If $V_c < V_r$, QA is reverse biased and the operation reverts to state 1.

State 3: Demagnetization through freewheeling. QA and D1 conduct, short circuiting the winding. The magnetic energy is discharged by a freewheeling current, and demagnetization proceeds slowly. Q1 has to withstand $V_c$.

State 4: Demagnetization by charging the capacitor. Both Q1 and QA are off. This winding is demagnetized through D1, capacitor $C$, and the input rectifier. The capacitor is charged by energy transfer from the winding and by the ac line. The energy $W_r$ returned from the winding is

$$W_r = (V_c - V_r) \int i_w(t)\, dt.$$

The total energy received by the capacitor is

$$W_c = V_c \int I_w(t)\, dt = \frac{V_c}{V_c - V_r} Wr. \tag{24}$$

Due to the four possible states, the inverter control is complex, while at the same time giving additional freedom in controlling the motor. The following comments apply:

- The capacitor voltage has to be kept within a relatively narrow band. Its minimum value, defined by the demagnetizing requirements, should be as high as possible. Its maximum value, on the other hand, determines the capacitor and thus all transistor ratings and should be as low as possible.
- For the capacitor to maintain an average constant voltage, the energy taken (state 2) must equal the energy given (state 4).
- During low-speed operation, the phase switches have to be PWM controlled, thus alternating between states 1 and 4. (The circuit operates then as a step-up chopper.) A rise in the capacitor voltage due to state 4 can be controlled by transferring the operation from state 1 to state 2.
- State 3 is used for demagnetization only at very low speeds when time is not critical. Providing that the capacitor is adequately charged, state 3 can be used during a PWM operation to permit reduced PWM frequency for the same ripple.
- During forced demagnetization (state 4), the switch QA has to be off until the current in that phase is reduced to zero. Table I summarizes the various states that can concurrently exist between the two adjacent phases.
- The motor maximum speed can be somewhat increased by using the higher capacitor voltage for part of the magnetizing cycle (state 2). However, a significant increase in the maximum speed is not possible since state 2 is used only to control the capacitor voltage, with the increase in the winding magnetizing voltage only secondary. The reason is that the

TABLE I
POSSIBLE CONCURRENT STATES

| | | Phase A | | | |
|---|---|---|---|---|---|
| | State | 1 | 2 | 3 | 4 |
| *P* | | | | | |
| *h* | 1 | Yes | No | No | Yes |
| *aB* | 2 | No | Yes | Yes | No |
| *s* | 3 | No | Yes | Yes | No |
| *e* | 4 | Yes | No | No | Yes |

capacitor does not have sufficient charge to sustain a phase current during a dwell period. If one tries to replenish this charge by a winding PWM control (boost-up chopper) at high speeds, one would reduce the total volt-seconds applied to the winding during the dwell period because of the chopper losses.

- The inrush current problem is eliminated since the capacitor is always pre-charged through one of the phases. This also means that the motor may rotate through a portion of a turn at each power-up.
- Since all active switches have to be capable of PWM operation, all gate drivers need to be adequately designed and all diodes should be of the fast type.
- With the dc link capacitor eliminated, the ac line is not buffered from the motor current pulses and line harmonics may be a problem.

To determine the rating of the inverter components, consider first that the minimum capacitor voltage necessary for a demagnetization has to be

$$V_c(\min) > \mathrm{CEMF} + V\sqrt{2} \tag{25}$$

where CEMF is the motor counter emf and $V$ is the line-to-line voltage, ac input. Thus, one needs to determine the motor CEMF. Consider first the dwell period $T_d$:

$$T_d = T_1 + T_c$$

where $T_1$ is the total time during which the rectifier line voltage $V_r$ is impressed across the winding (state 1) and $T_c$ is the total time during dwell when the capacitor voltage is impressed across the phase winding (state 2). Then,

$$CEMF = \frac{T_c \times V_c + T_1 \times V_r}{T_d} = m_1 \times V_r + (1 - m_1) V_c \tag{26}$$

where $m_1$ is the rectified voltage duty cycle during the dwell period. The total energy given to the winding during the dwell is

$$\begin{aligned} W_t &= T_d \times \mathrm{CEMF} \times I_w \\ &= T_d[m_1 \times V_r + (1 - m_1)V_c] \times I_w = W_{1m} + W_{cm} \end{aligned} \tag{27}$$

where $W_{lm}$ and $W_{cm}$ are the energies transferred to the motor from the ac line and the capacitor, respectively.

During demagnetization, the motor returns to the capacitor a portion $X$ of the total energy $W_t$:

$$W_r = X \times W_t = X \times T_d \times \mathrm{CEMF} \times I_w. \tag{28}$$

The total energy transferred to the capacitor is

$$W_c = W_r + W_{1c} \tag{29}$$

where $W_{1c}$ is the energy supplied by the ac line to the capacitor. Also from (24),

$$W_c = \frac{W_r \times V_c}{V_c - V_r} = \frac{X \times T_d \times I_w \times \text{CEMF} \times V_c}{V_c - V_r} \tag{30}$$

$$W_{lc} = \frac{X \times T_d \times I_w \times \text{CEMF} \times V_r}{V_c - V_r}. \tag{31}$$

The capacitor energy is constant so that the energies supplied and received must be equal:

$$W_c = W_{cm}. \tag{32}$$

Also, the energy is supplied by the line and converted into mechanical work:

$$W_1 = W_{1m} + W_{1c} = W_n = (1 - X)W_t \tag{33}$$

From (32) and (33) it follows that

$$\frac{X \times V_c}{V_c - V_r} = (1 - m_1) \times \frac{V_c}{\text{CEMF}} \tag{34}$$

$$\frac{X \times V_r}{V_c - V_r} + m_1 \times \frac{V_r}{\text{CEMF}} = 1 - X \tag{35}$$

from which one obtains the maximum motor voltage:

$$\text{CEMF} = \frac{V_r}{1 - X}. \tag{36}$$

The last expression is simplified by replacing the rectified voltage $V_r$ by $V_{\text{dc}}$. From (25), the capacitor rating, with the voltage ripple included, is

$$V_c(\text{min}) = \left(\frac{V\sqrt{2} + V_{\text{dc}}}{1 - X}\right)(1 + DV). \tag{37}$$

Equations (36) and (37) indicate that an increase in returned energy $X$ allows a higher motor speed for the same ac line voltage while increasing the capacitor voltage rating at the same time. Using a typical value $X = 0.25$, the voltage rating becomes

$$V_c(\text{min}) = 2.27V\sqrt{2}(1 + DV) \tag{38}$$

The capacitor minimum value is

$$C_{\min} = \frac{W_r}{2.27V \times DV\sqrt{2}} \tag{39}$$

where $W_r$ is defined by (10a). The capacitor size is normally determined by its rms current rating. First,

$$\text{CEMF} = m_c \times V_c + (1 - m_c) \times V_{\text{dc}} \tag{40}$$

where $m_c$ is the modulation index of QA and can be calculated for a worst-case condition from (36) and (40). The capacitor rms current is then

$$I_{\text{rms}}C = \sqrt{I_a^2 + m_c \times (I_{w\text{rms}}^2 - Iw_{\text{dc}}^2)} \tag{41}$$

where $I_a$ is the ac component of current tails during demagnetization.

To determine the current rating of QA, consider the motor just starting. Assume that Q1–QN are PWM controlled with a 50% duty cycle and that QA is also operating with a 50% duty cycle (to allow for demagnetization). Assume that there is a dwell overlap and that each operating phase draws the full peak current $I_{pw}$. The tail current from the two phases charging the capacitor are $0.5I_{pw}$ and $0.5I_{pw}$.

The capacitor is discharged with an equal current of $I_{pw}$, which passes through QA. Since QA operates with a 50% duty cycle, its peak current is $2I_{pw}$. As a result, the inverter device ratings are

| | |
|---|---|
| Voltage rating, all devices | $2.27V\sqrt{2}(1 + DV)$ |
| Current rating, Q1–QN and D1–DN | $I_{pw}$ |
| Current rating QA and DA | $2I_{pw}$ |
| kVA rating, active devices | $2.27(N + 2) \times I_{pw} \times V\sqrt{2}(1 + DV)$ |

### F. Summary

The general discussion presented in this section indicates that all dual-rail inverters suffer from a requirement for a minimum voltage rating of approximately twice the motor supply voltage. For that reason, single-rail inverters (Fig. 1(a), (b)) will, most likely, be the choice for 380-V and 460-V industrial SRM drives. Of these two, the Miller inverter (Fig. 1(b)) is clearly preferred if the restriction posed by a current overlap can be resolved. (There is no restriction for the overlaps occurring below the speed at which the available demagnetizing voltage is approximately equal to the magnetizing voltage.)

Finally, note that the circuit comparison based on the required inverter kVA is only one of the criteria to be used and that one, after narrowing the choice, should do a more detailed analysis to justify the final selection.

## IV. Numerical Example—High-Speed Drive

In order to illustrate the design procedure given in Section III, we present a design for a high-speed drive. The design is carried out for each circuit given in Fig. 1. The ac line supply voltage is 380 V, 50 Hz. The drive uses a high-speed, unsymmetrical 6/2 motor [8], schematically shown in Fig. 2 and suitable for spindle applications. The motor used in this example has the following characteristics:

Four low sped poles, with 120 turns per pole
Two high speed poles, with 70 turns

| | |
|---|---|
| Base speed | 3100 rpm |
| Maximum speed | 20 000 rpm |
| Rated power | 10 kW |
| Rated torque | 30.8 Nm |
| Rated rms current | 47.5 A |
| Rated peak current | 111 A |
| Rated efficiency | 86% |

In order to achieve the desired speed range, 0–20 000 rpm (Fig. 8), the motor control strategy requires special attention.

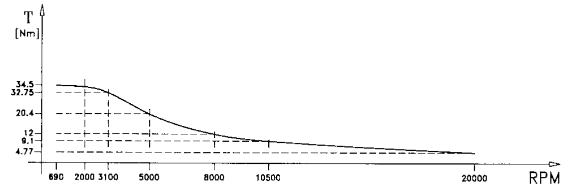


Fig. 8. Speed-torque boundary of the 10-kW 6/2 motor.

As discussed in Section II, symmetrical SRM's are ill suited for constant-power operation over an extended speed range, since, with a fixed dwell angle and a constant supply voltage, the motor power becomes inversely proportional to the speed.

To reconcile the high- and low-speed requirements, one needs to modify the motor configuration as the speed is increased [8]. Fortunately, SRM's are amenable to such an approach and the 6/2 geometry offers several alternatives. In this case, a high-speed winding, placed on the third phase, permits one to practically double the motor speed from 10 500–20 000 rpm. Table II gives information about the key motor operating points in the intended speed range. These points are then used in the design of the drive inverters. The following comments apply:

1) With a 6/2 motor, the torque at a standstill is typically produced by only one pole pair. Furthermore, this torque greatly depends on the rotor position. For the worst-case scenario, the nominal torque at standstill requires 208 A in the two low-speed windings and 217 A in the high-speed winding. An inverter rated for these starting currents would obviously be oversized and uneconomical. Given the high-speed application of the 6/2 motor, the decision was made to restrict the starting currents to nominal peak value and to design all inverters accordingly. The worst-case starting torque is therefore reduced to 11 Nm or 37% of the nominal torque. Note that, statistically, the starting torque will be higher, but 11 Nm is the absolute minimum value.

2) In considering motor control, a full demagnetization voltage of 515 V is assumed. Any reduction of this voltage will change the ratio between dwell and conduction angles, resulting in decreased torques.

3) At low speeds, the high-speed winding is inefficient and is switched off as soon as the motor has started.

4) From standstill to 5000 rpm, the magnetizing voltage is gradually increased until all available voltage is used. However, at 5000 rpm, the dwell angle is very short (the optimum dwell angle is approximately 67°) and the currents are relatively small. With the available magnetizing voltage fully utilized, the dwell angle is increased to maintain constant power from 5000–8000 rpm.

5) At 8000 rpm the operation is switched to a 2/2 configuration with a low-speed winding, primarily to maintain drive efficiency.

6) At 10 500 rpm a switch to the high-speed winding results in a lower inductance, permitting a decrease in the current advance and a reduction of the current peaks. At the same time, the applied voltage can be reduced, leaving room for a further speed increase.

7) At 20 000 rpm, the motor is using all available voltage and is operating close to its maximum dwell angles. A further increase in speeds would result in a reduction of the output power.

8) For control giving the same dwell and conduction angles to each phase, the current overlap exists at every point below 8000 rpm except point 2.

9) In the inverter design, each component is rated to enable the drive operation at each point listed in Table II, except for circuit 2, for which new operating points are defined in order to avoid the current overlap.

With the motor load defined, the inverter design is performed using the procedure outlined in Section III. First, taking into account the motor efficiency and using $X = 0.25$, the line rectifier and the dc link filter are:

| | |
|---|---|
| Rectifier | $P_n = 11.625$ kVA |
| from (7) | $I_{dc} = 22.5$ A |
| | $I_{rms}L1 = 27.6$ A |
| from (8c) | $I_{rms}C = 80$ A |
| from (9) and (11) | $C_{min} = 353$ $\mu$F |

The numerical design is carried for each circuit of Fig. 1. A 5% current ripple $R$ and a 20% voltage ripple $DV$ are assumed throughout the design.

### A. Circuit 1: Classic Inverter

| | |
|---|---|
| From (10a) | $W_r = 18.75$ J |
| From (11) | $V_pQ = V_pD = 645$ V |
| From point 4, Table II | $I_pQ = 111$ A |
| The kVA, active devices | 429.6 kVA |

### B. Circuit 2: Miller's Inverter

Since this circuit has restrictions with respect to current overlaps, the motor control shown in Table II has to be modified in the range of 2000–8000 rpm. First, below 2000 rpm, the magnetizing voltage ($VY$, Fig. 1(b)) is always less than half the dc-link voltage and the overlap does not pose a problem. From 2000–8000 rpm one should control the motor in the following way:

1) From 2000 to 5000 rpm the motor operates in a 4/2 configuration with a partial tail overlap. When there is no overlap, the demagnetizing voltage is 515 V. During the overlap, the average demagnetizing voltage is reduced by the value of the magnetizing voltage and is given in parenthesis in Table III.

2) From 5000 to 8000 rpm, the phase dwell angles are controlled unsymmetrically to avoid the overlap. To illustrate, assume that in Fig. 2, phase A is the high-speed (not used) phase and that the rotor is turning clockwise. Then phase B is controlled with a wide dwell angle and phase C with a narrow angle. As the speed approaches 8000 rpm the contribution of phase C decreases until, at 8000 rpm, phase C is disconnected and the motor continues in the 2/2 configuration with phase B. From then on, the motor is controlled as in Table II.

Table III defines the modified operating points for the inverter circuit 2. The ratings of all components for circuit 2 are the same as for circuit 1 except for the chopping switch

TABLE II
OPERATING POINTS AND CONFIGURATIONS FOR THE 6/2 MOTOR

| Quantity \ Point | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| Speed, rpm | 0 | 690 | 2000 | 3100 | 5000 | 8000 | 8000 | 10 500 | 10 500 | 20 000 |
| Configuration | 6/2 | 4/2 | 4/2 | 4/2 | 4/2 | 4/2 | 2/2 Slow | 2/2 Slow | 2/2 Fast | 2/2 Fast |
| Magnet/demagn. voltage, volts | 15/515 | 102.4/515 | 241/515 | 391/515 | 515/515 | 515/515 | 441/515 | 515/515 | 398/515 | 515/515 |
| Dwell/conduct. angles | 90/95 | 50/57 | 46/69 | 38/64 | 36/72 | 54/108 | 67/112 | 72/144 | 59/107 | 69/137 |
| Phase peak current, A | 111 | 101 | 101.5 | 111 | 92.9 | 85.76 | 104 | 110 | 108.5 | 104 |
| Phase rms current, A | 78 | 45.7 | 44.5 | 47.5 | 38 | 33.42 | 45.7 | 54 | 50 | 46.9 |
| Total torque, Nm | 11[a] | 34.5 | 34.25 | 32.75 | 20.4 | 12.75 | 12 | 9.1 | 9.1 | 4.77 |
| Total power, W | 0 | 2492 | 7173 | 10 631 | 10 681 | 10 681 | 10 053 | 10 005 | 10 005 | 10 000 |
| Returned energy ratio, $X$ | | 0.21 | 0.24 | 0.23 | 0.25 | 0.22 | 0.19 | 0.23 | 0.2 | 0.19 |

[a]Worst-case rotor starting position.

TABLE III
POINTS WITH MODIFIED CONTROL FOR CIRCUIT 2

| Quantity \ New Point<br>Speed, rpm | Phase | 4a<br>3100 | 5a<br>5000 | 5b<br>5000 | 6a<br>8000 |
|---|---|---|---|---|---|
| Magnet/demagn. voltage, V | B | 242/515(274) | 257/515(258) | 277/515 | 398/515 |
| | C | Same | Same | 515/515 | 515/515 |
| Dwell/conduct, angles | B | 55/101 | 67/130 | 67/107 | 67/118 |
| | C | Same | Same | 23/46 | 23/46 |
| Peak current, A | B | 114 | 95 | 105 | 98 |
| | C | Same | Same | 110 | 101 |
| RMS Current, A | B | 51 | 42.2 | 46 | 42.6 |
| | C | Same | Same | 41.2 | 39.58 |
| Returned energy ratio, $X$ | B | 0.21 | 0.24 | 0.2 | 0.22 |
| | C | 0.21 | 0.24 | 0.24 | .23 |
| Torque, Nm | B | 15.5 | 9.87 | 11.85 | 9.5 |
| | C | 15.5 | 9.87 | 8.15 | 2.5 |
| Total power, W | | 10 063 | 10 335 | 10 471 | 10 053 |

QA and the diode DA that must be rated for $2I_{pw} = 222$ A to provide the overlapping starting currents. The total kVA of the active devices for the Miller's inverter is 357.9 kVA.

### C. Circuit 3: Buck-Boost Inverter

This circuit has no overlap restriction so that the control defined in Table II is used.

| | |
|---|---|
| From (12a) | $I_{dc}DA = 222$ A |
| From (12b) | $I_{dc}L2 = 233.6$ A |
| From (13b) | $I_pQA = 239.7$ A |
| From (14) | $I_{rms}L2 = 234$ A |
| From (15a) | L2 = 2.8 mH |
| C1(min) is the same as for Circuit 1 | |
| From (18) | $C_2(\min) = 141\ \mu$F |
| The total kVA for active devices | 738.7 kVA |

### D. Circuit 4: C-Dump Inverter

The ratings of all phase switches Q1–Q3 and the feedback diodes D1–D3 is the same as in the buck-boost inverter. The rating of L2 is the same as that for L1 in the dc-link filter. The minimum value for the dc-link capacitor C2 is

| | |
|---|---|
| From (21) | C2(min) = 706 $\mu$F |
| From (22) | $I_pQA = 233.1$ A |
| The kVA rating, all active devices | 730 kVA |

### E. Circuit 5: Sood's Inverter

The current rating of the phase switches Q1–Q3 and the diodes D1–D3 is the same as for the other inverter (111 A). The current rating for QA and DA is 222 A. The voltage rating for all devices, from (38) is 1462 V. The total kVA for the active devices is 812.8 kVA.

### F. Discussion

From the numerical results one draws the same conclusion as in Section III: if the current overlap restriction can be resolved, circuit 2, Fig. 1(b), gives the most economical topology. The dual-rail circuits are penalized by the required high-voltage rating and are not justified in industrial drives supplied from a 380- or 460-V ac line.

## V. NUMERICAL EXAMPLE: HIGH-TORQUE DRIVE

The design procedure given in Section III is used here to evaluate numerically the suitability of the five, four-phase inverter circuits (Fig. 1) for a low-speed high-torque drive. The drive uses a 8/6 motor, schematically presented in Fig. 3, with the following characteristics:

| | |
|---|---|
| Number of phases | 4 |
| Rated voltage | 510 V |
| Rated peak current | 63.35 A |
| Rated rms current | 26.12 A |
| Rated speed | 30 000 rpm |
| Rated torque | 31.83 Nm |
| Rated power | 10 kW |

The motor is controlled with a dwell angle of 13 and a conduction angle of 26°, which leads to a current overlap. The dwell angle is reduced to 8°, in the case of circuit 2, in order to eliminate the overlap, leading to an inefficient design, which is included here only for comparison.

The numerical results for the key inverter components are summarized below. A 5% current and 20% voltage ripple are assumed and each inverter circuit of Fig. 1 is modified to include four phases. As in the previous example, the phase-starting current is limited to its peak rated value (63.35 A), giving a starting torque of approximately 17 Nm for the worst-case rotor initial position.

### *A. Circuit 1: Classic Inverter*

| | |
|---|---|
| Voltage rating, all devices | 645 V |
| Current rating, all devices | 63.85 A |
| Total kVA, active devices | 329.5 kVA |

### *B. Circuit 2: Miller's Inverter*

Since the dwell angle has to be reduced to 8° to avoid the current overlap, the currents are increased so that the peak current for each phase becomes 137 A. The device ratings are then:

| | |
|---|---|
| Voltage rating, all devices | 645 V |
| Current rating, phase switches | 137 A |
| Current rating, chopper switch | 274 A |
| Total kVA, active devices | 530 kVA |

### *C. Circuit 3: Buck-Boost Inverter*

| | |
|---|---|
| Voltage rating, all devices | 1290 V |
| Current rating, phase devices | 63.85 A |
| Current rating, chopper devices (QA and DA) | 137.9 A |
| Total kVA, active devices | 507.3 kVA |

### *D. Circuit 4: C-Dump Inverter*

| | |
|---|---|
| Voltage rating, all devices | 1290 V |
| Current rating, phase devices | 63.85 A |
| Current rating, chopper devices (QA and DA) | 134 A |
| Total kVA, active devices | 502.3 kVA |

### *E. Circuit 5: Sood's Inverter*

| | |
|---|---|
| Voltage rating, all devices | 1463 V |
| Current rating, phase devices | 63.85 A |
| Current rating, chopper devices (QA and DA) | 127.7 A |
| Total kVA, active devices | 560.4 kVA |

From these results, the classic inverter, circuit 1, is the clear choice. In fact, none of the other circuits could really be used in this application. Circuit 2 is not good because it leads to poor inverter and motor utilization with too-narrow dwell angles; all other circuits with dual-rail topology are not applicable because of the unacceptable voltage ratings.

It is interesting to compare the required inverter kVA for the 6/2 and 8/6 motors, which leads to a tentative conclusion that low-speed motors require less "peaky" currents and, thus, for the same motor power, require less installed inverter kVA.

## VI. Experimental Results

The experiments were performed with the inverter circuits (Fig. 1) nos. 1 (classic), 2, 3, and 5, on the high-torque experimental 8/6 motor. The dimensions of the stator and rotor poles are given in Fig. 9. The motor parameters are as follows:

| | |
|---|---|
| Axial length | 139 mm |
| Rotor diameter | 103 mm |
| Airgap | 0.3 mm |
| Number of turns per pole | 28 |
| Resistance per phase | 70 mΩ |
| Aligned inductance at 50 mA | 15.1 mH |
| Nonaligned inductance at 50 mA | 2.24 mH |
| Rated power | 1600 W |

The motor was loaded appropriately and the starting (Θs) and the dwell angles were adjusted to obtain the minimum current at each test point. The measured waveforms are shown in Figs. 10–13 and the results are grouped in Table IV.

The following comments apply:

1) Circuit 2 is inappropriate for the 8/6 motor because of the current overlap restriction. To prevent the overlap, the dwell angle was restricted to 8° and the current tail was 7°. The motor supply voltage had to be raised 50% to 305 V in order for the motor to deliver the required 1.6-kW power. The effect on the current pulse width is clearly seen in Fig. 11(b).
2) At this operating point, the 2-kHz PWM control was used only on switch QA (Fig. 1(c) and (e)) to control the capacitor voltage. Because, in the case of circuit 5 the capacitor discharges through the motor winding, the PWM operation is present in the motor currents (Fig. 13).
3) The capacitor-discharge current is highly distorting the input current in circuit 5 (Fig. 13(b)).

## VII. Conclusion

The paper described two new inverter circuits, which were not published before, and gave a detailed design procedure for the five circuits that were considered. Of these five, only two circuits were found suitable for industrial SRM drives supplied from 380 or 460 V ac lines. The remaining three circuits all use dual-rail topology and thus require that the inverter-active devices have a rating at least twice the motor supply voltage. Consequently, the dual-rail inverters may find applications in low-power low-voltage drives but are not suitable for industrial drives.

If the current overlap (interval over which the two phases conduct concurrently) can be restricted to speeds where the motor-magnetizing voltage is below approximately one half the dc-link voltage, the most advantageous circuit is the one reported by Miller [7]. However, since the majority of

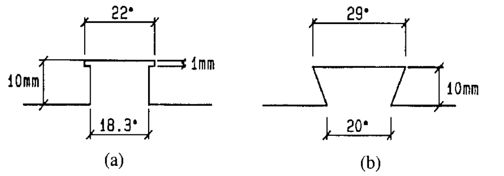


Fig. 9. Details of the 8/6 motor: (a) Stator pole; (b) rotor pole.

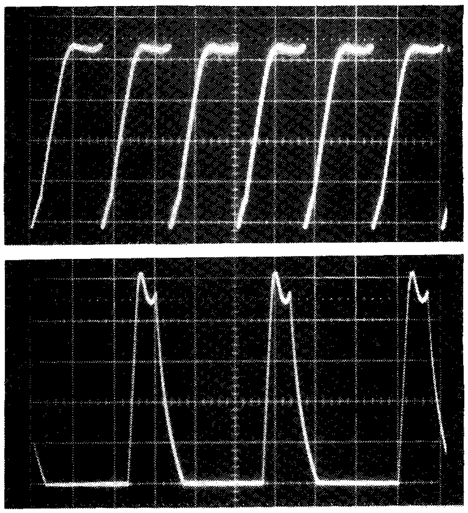

Fig. 10. Circuit 1 (classic inverter). Upper: dc-link current, 10 A/div and 0.5 ms/div. Lower: winding current, 5 A/div and 1 ms/div.

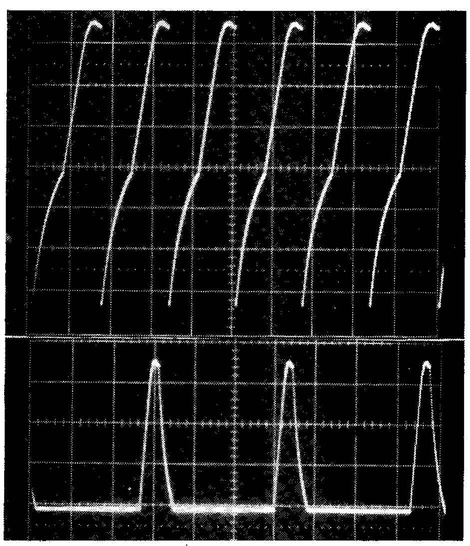

Fig. 11. Circuit 2. Upper: dc-link current, 10 A/div and 0.5 ms/div. Lower: winding current, 10 A/div and 1 ms/div.

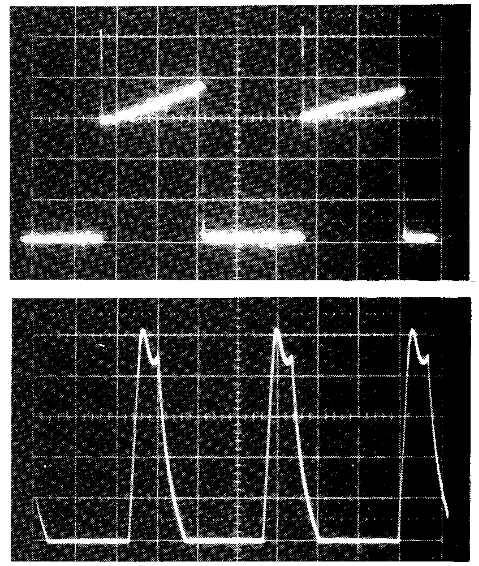

Fig. 12. Circuit 3 (buck-boost inverter). Upper: current, QA chopper, 1 A/div and 0.1 ms/div.

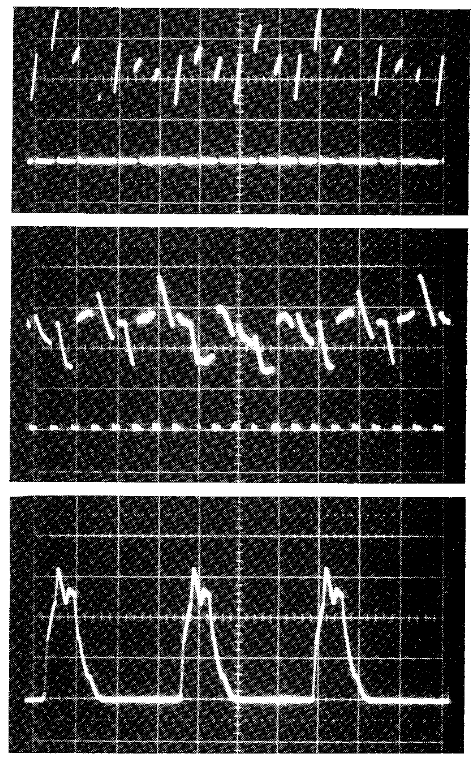

Fig. 13. Circuit 5. Upper: current, QA chopper, 10 A/div and 0.5 ms/div. Lower: winding current, 10 A/div and 1 ms/div.

SRM's operate with a current overlap over most of their speed range, the "classic" inverter (Fig. 1(a)) becomes the most attractive topology in that case.

The SRM starting torque very much influences the inverter rating. In order to provide a rated torque starting for any rotor position, the inverter rating may have to be increased several times over the value required by the motor-rated power. Conversely, if the starting currents are limited to their rated value, the starting torque is severely reduced for worst-case rotor initial position.

TABLE IV
SUMMARY OF EXPERIMENTAL RESULTS

| Inverter \ Variable | $V_{dc}$, V | Dwell | $I_{dc}$, A | $I_{dc}$rms, A | $I_{wp}$, A | $I_{wrms}$, A | $I_pD$, A | $I_p$QA, A | $I_{rms}$QA, A | $I_p$DA, A | $I_c$, A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1: classic | 200 | 13 | 18.6 | 23.5 | 25.6 | 10.45 | 23.5 | — | — | — | 16.3 |
| 2: circuit | 305 | 8 | 7.81 | 22.6 | 36.1 | 11.3 | 24 | 36.1 | 19.8 | 35 | 22 |
| 3: buck boost | 195 | 13.3 | — | — | 26 | 10.5 | 22.57 | 40 | 21.6 | 40 | 16.73/17.1 |
| 5: circuit | 210 | 13.3 | 19.95 | 24.11 | 34.7 | 12.52 | 34.1 | 40.5 | 14.7 | — | 14.6 |

$p$ = peak value, $w$ = winding, QA/DA = chopper switch/diode, and $D$ = phase diode.

The need for a high PWM frequency is not as strong in SRM drives as in induction motor drives because the inverter output "sees" the total phase inductance—not only the leakage inductance as with the induction motors. That, combined with the freewheeling inverter states, permits reduced PWM frequency for the same current ripple.

Finally, regardless of the technical merits of the SRM technology, an industrial use of SRM's in general-purpose drives is most unlikely given the need for an extremely close design coordination between the motor, the control and the inverter. That coordination has to be much closer than in the case of brushless drives and indicates that SRM applications may be more successful if directed toward unique, special-purpose or OEM-type drives.

## ACKNOWLEDGMENT

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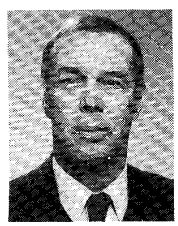

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