SRM INVERTER TOPOLOGIES: A COMPARATIVE EVALUATION

S. VUKOSAVIĆ and **V.R. STEFANOVIĆ**

INSTITUTE "Nikola Tesla"
Viktora Igoa 3
11000 Beograd
YUGOSLAVIA

SIEI PETERLONGO
Via Carducci, 24
21040 Gerenzano, VA
ITALY

Abstract

Several inverter power circuits, suitable for switched reluctance motor (SRM) drives are analyzed and are compared with each other. The comparison is based on the peak voltage and current ratings of power switches and on the size and peak ratings of the DC link components. Since the converter choice depends on the motor design, the converter analysis and selection are done for a high speed, 6/2 SRM, suitable for a spindle drive and a high torque, 8/6 motor. Experimental results obtained for a high torque drive are included.

1. INTRODUCTION

Although the SRM drives have not yet found broad industry acceptance, they continue to attract research interest, stimulated mainly by the promise of a simple and rugged motor construction, the possibility of high motor speeds, high torque to inertia ratio, an inverter with a reduced number of power switches and an overall robust drive. This research activity has resulted in a number of inverter topologies, some of which have been described in the literature [1-5]. However, although a comparison of the required kVA ratings between a SRM and an induction drive inverter was done [6], no comparison exists between different inverter topologies which are suitable for an industrial SRM drive.

This paper considers five inverter circuits, represented in Fig. 1., with the objective of establishing the most appropriate topology for an SRM drive. Although there are other inverter circuits which could be used for this application, the five circuits considered here are possibly the most promising. Note also that inverters for motors with bifilar windings are not considered in this study.

As the study progressed, it became evident that the suitability of a particular inverter circuit changes with the motor geometry, making an absolute, general choice impossible. Note that this is in contrast with drives operating with sinusoidal voltages or currents, where the inverter topology is independent of the motor design. Specifically, in the case of SRMs, it was found that the number of the stator/rotor poles and the related issues of the dwell angle and current overlap (current being injected into one phase, while the adjacent phase current is still flowing) affect the inverter choice. For that reason, the study was expanded to include a high-speed, 6/2 motor, presented in Fig. 2. and a high torque, 8/6 motor, shown in Fig. 3. These two drives are then examined separately and the most suitable inverter circuit for each one is identified. As it will be seen, the key parameter affecting the inverter selection is whether a motor operates with or without an overlapping current through its speed range. Thus, although based on two motor geometries, the analysis presented in this paper can be generalized to all SRMs, by using the current overlapping as a dividing criterion.

In the next section, principles of a motor operation are briefly examined in order to define the requirements for a SRM inverter. Following that, the operation of each inverter circuit, presented

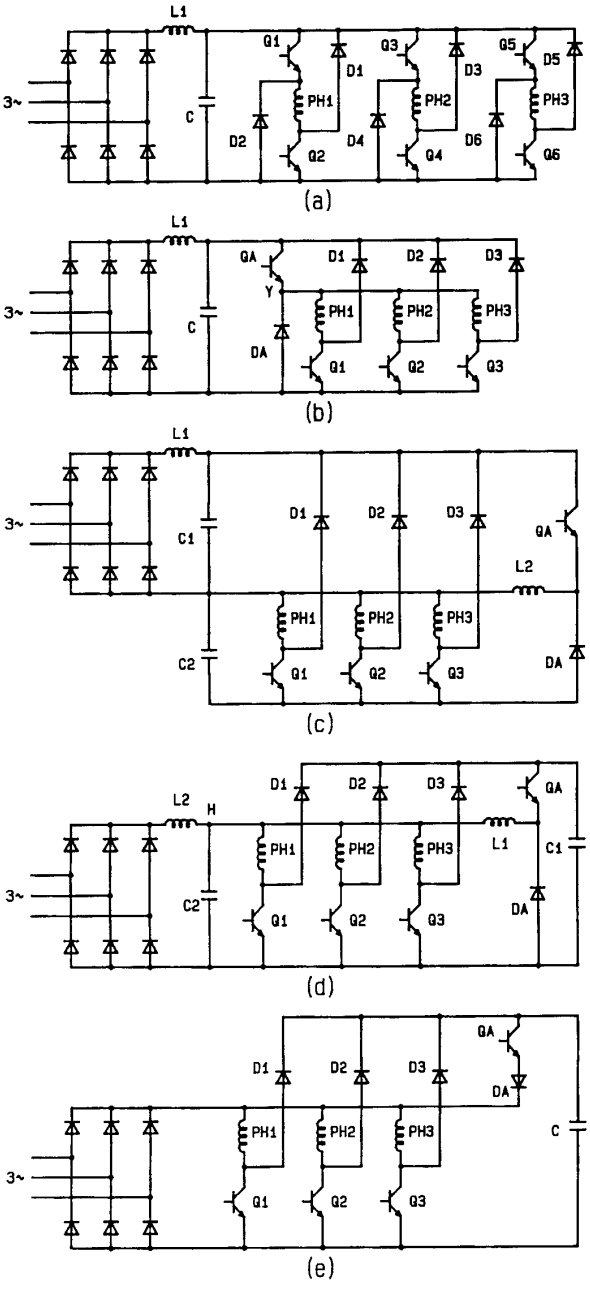

Fig. 1.: The five circuits analyzed in this study.
a) No. 1, "classic" inverter
b) No. 2 circuit
c) No. 3, Buck-Boost inverter
d) No. 4, C-dump inverter
e) No. 5, reduced component inverter

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in Fig. 1. is described, the equations for a selection of circuit components are identified, the inverter total kVA rating is determined, and the inverter suitability is evaluated against the requirements defined by motor operation.

After that, the power components of the five inverters, Fig. 1., are chosen for a 10kW drive, first for the 6/2 and then for the 8/6 motor. The most suitable inverter circuit is then selected, primarily by considering the total required VA inverter rating.

Finally, experimental results, obtained with the 8/6 drive and the inverter circuits from Fig. 1. are presented.

2. BASIC MOTOR REQUIREMENTS

The material given in this section is available in the literature and is included here only for the sake of completeness and in order to define the required inverter characteristics.

Unlike in machines with distributed windings, the energy conversion in SRMs occurs in discrete cycles (sometimes called strokes), through the interaction of one stator and one rotor pole pair. Fig. 4. shows a typical change in the stator self-inductance as a function of rotor position, while Fig. 5. defines the corresponding angles. The flat portion of the Lmax curve (dead zone, [1]), Fig. 4., is caused by a difference in width of the stator and rotor poles. It is normally provided so that negative torques can be avoided during demagnetization. The stator poles are normally made more narrow, to leave sufficient space for the winding.

The winding is usually switched to a voltage source at an angle equal or smaller than Θ1, giving rise to a stator current, Fig. 6. The current waveform depends on the motor speed, the forcing voltage, the winding total inductance, and the turn-on angle Θs.

At Θ=Θ2 the polarity of the voltage connected across the motor phase is reversed and a demagnetization begins. The waveform of the resulting current tail, Θ2-ΘE depends on the forcing voltage, the energy stored and the motor speed. If the current flows beyond Θ=Θ3, a negative torque is generated, Fig. 6b. The current and torque waveforms, Fig. 6., are qualitative only and will vary with the motor operating conditions and the motor geometry.

Under certain conditions, the energy conversion process may occur simultaneously in two adjacent phases, causing a current overlap, Fig. 7. As will be seen later, the existence of the overlap at high motor speeds eliminates some inverter circuits from consideration.

It is obvious from Fig. 4 that the motor torque can be increased by widening the range Θ1-Θ2, where the inductance change, dL/dΘ, has a positive slope. Since dL/dΘ is proportional to the width of a stator pole, this leads to a motor design with wide stator poles. On the other hand, wide poles lead to a current overlap while at the same time, due to increased inductance, limit the motor speed range for a given supply voltage.

It is instructive to establish the limit conditions for a current overlap. Denote by Ns and Nr the number of stator and rotor poles respectively, by PW the width of the stator pole and by K1 the ratio of a stator pole width and a pole-pitch. Assuming that the rotor poles are wider or equal to the stator poles, the stator pole

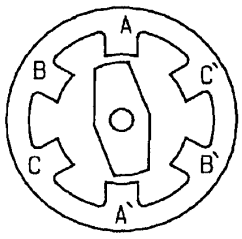

Fig. 2.: High speed 6/2 SRM

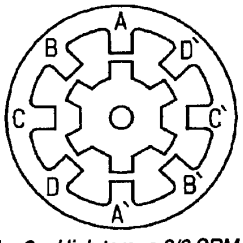

Fig. 3.: High torque 8/6 SRM

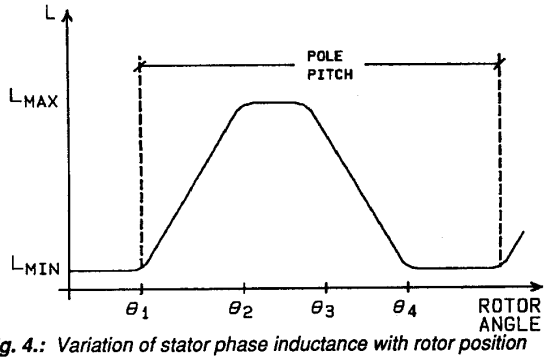

Fig. 4.: Variation of stator phase inductance with rotor position

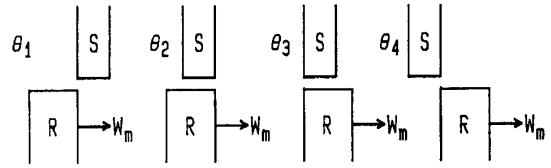

Fig. 5.: Definition of rotor angles

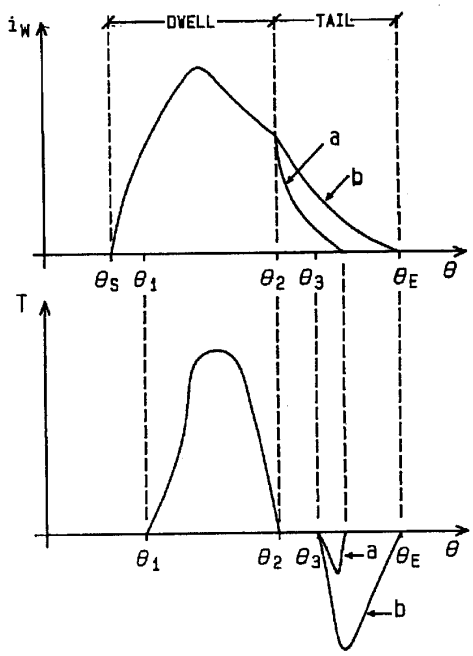

Fig. 6.: Qualitative representation of current and torque during one energy cycle. Negative torque is produced when current flows past Θ = Θ3

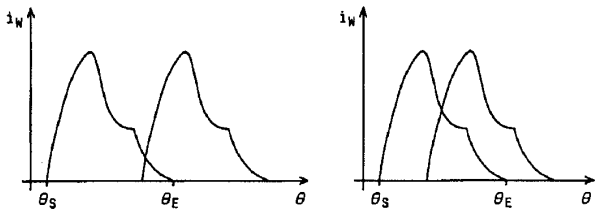

Fig. 7.: Definition of the current overlaps
a) tail overlap
b) dwell overlap

width is:

$$PW = 360 * K1/Ns$$

The pole width, PW is equal to the arc over which $dL/d\Theta$ is positive. Denote by K2 the ratio between the width of the current pulse, $CW = \Theta S - \Theta E$, Fig. 6., and the width of the arc over which $dL/d\Theta$ is positive, so that:

$$CW = (K2) * (PW) \quad (1)$$

On the other hand, the number of current pulses per one turn is N * Nr. The width of this pulse is 360/(N * Nr). Obviously, then, the limit of a current overlap exists if:

$$360/(N * Nr) \geq 360 * K1 * K2/Ns$$

From which it follows that the limiting width of the current pulse is:

$$K2 \leq Ns/(N * Nr * K1) \quad (2)$$

As an example, assume that the stator pole occupies half of the pole-pitch, K1 = 0.5. For 8/6 geometry, eq. (2) gives $K2 \leq 1$, which is impractical. (To avoid overlap, the current should flow only when $dL/d\Theta$ is positive, eq. (1)). The same result is obtained for a 6/4 motor. The 6/2 motor gives $K2 \leq 2$, which is realistic and acceptable, after the motor has started.

This discussion indicates that most SRMs operate with a current overlap. One needs then to do a detailed verification to determine if a given inverter circuit can provide the necessary voltages in the speed range when a current overlap exists.

Consider briefly now the issue of the motor constant power range. As the motor speed is increased, the time available for winding magnetization tm, decreases:

$$tm = DWELL/w \quad (3)$$

If V is the magnetizing voltage, the flux per pole is:

$$\phi = k * tm * V = k * DWELL * V/w$$

Since SRMs are single excited machines, the torque is proportional to:

$$T = ko * \phi^2 = ko\ (DWELL * V/w)^2 \quad (4)$$

while the motor power is:

$$P = k'/w \quad (5)$$

From (4) and (5) it is clear that SRMs are not well suited for operation over a wide speed range above the rated speed. The situation is improved by using a motor with low speed windings, having a large number of turns and, in the other phase, a high speed winding with a small number of turns. While such a motor will have somewhat higher current at starting in the high speed winding, its speed range would be considerably increased. Such an approach is used on the 6/2 motor, Fig. 2., which is further described in section 4.

From this discussion one can formulate some functional requirements that a SRM inverter should ideally meet:

1. It needs to control the voltage applied to the winding at low speed, so as to limit the winding current. Either voltage or current PWM control can be used.
2. It needs to have sufficiently high forcing voltage, at each operation point, so that the current is injected sufficiently quickly into the winding, Fig. 7. Obviously, this requirement is critical at high speeds, since the time available is decreased, t = DWELL/w.
3. It has to have as high a demagnetizing voltage as possible, in order to shorten the current tail, thus avoiding negative torques and/or permitting an extension of the dwell angle, Fig. 6.
4. It has to provide independent control of phase currents in motors having current overlap, Fig. 7., so that energy can be supplied to one phase while extracting it simultaneously from the other phase.
5. It has to provide an efficient energy recycling during a demagnetizing interval. This is an important requirement given the highly cyclical energy exchange between the inverter and the motor.
6. It should isolate the AC network from the current pulse shocks caused by the motor. On the other hand, with a three-phase AC supply, the motor is practically insensitive to the rectifier output ripple.

Finally, one should note that the inverter current rating is determined by the starting torque requirements, while the voltage rating is fixed by the maximum motor speed. Specifically, in the next section, current overlap is assumed at starting and each inverter circuit is dimensioned accordingly.

3. INVERTER CIRCUITS

Before the five circuits, Fig. 1., are discussed, it is useful to divide all SRM inverters into two groups:

- single rail inverters
- dual rail inverters.

The single rail circuit is characterized by having one voltage available for magnetizing and demagnetizing of the motor phases. In the dual rail circuit, two voltages are used. In Fig. 1., (a) and (b) are the single rail inverters while (c), (d) and (e) are the dual rail inverters.

Each inverter is now described and the procedure to calculate the circuit elements is presented. In order to avoid confusion and to preserve a level playing field, the calculations and the numerical values in sections 4 and 5, do not include the normal design margins nor do they include the rounding of the calculated

values to the nearest available component value.

The following notation is used in the calculation of inverter components:

N - number of motor phases
Ns - number of stator poles
Nr - number of rotor poles
wn - base (rated) motor speed, rad/sec
CEMF - motor counter electromotive force, Volts
V - input AC line-to-line RMS voltage, Volts
Vdc - rectified DC voltage, $Vdc = 3V\sqrt{2}/\pi$, Volts
DV - relative increase of the capacitor voltage
Ipw - peak value of the phase winding current, Amps
Irmsw - RMS value of each phase current, Amps
Wt - total energy a winding receives during a DWELL period
X - percentage of Wt returned to the inverter, $0<X<1$
Wr - energy returned to the inverter during demagnetization

$$Wr = X * Wt \qquad (6a)$$

P - power to which the inverter is designed, Watts
Pn - portion of the motor input power converted to mechanical work, Watts

$$P = Pn/(1 - X) \qquad (6b)$$

CALCULATION OF THE INPUT RECTIFIER AND THE DC LINK FILTER:

$$Idc = P/Vdc \qquad (7)$$

selecting the DC link choke so that the DC link current is at a limit of continuous conduction at rated load, one has:

$$Ip = IpL = 2 * Idc \qquad (8a)$$

where Ip and IpL are the peak currents of the input rectifier and the DC choke, respectively. The choke RMS current is:

$$IrmsL = 1.227\ Idc \qquad (8b)$$

The DC link capacitor is normally determined on the basis of its RMS current:

$$IrmsC = \sqrt{(IrmsL)^2 + N(Irmsw)^2 - 2(Idc)^2} \qquad (8c)$$

However, the capacitor value should not be smaller than:

$$Cmin = Wr/(DV * Vdc^2) \qquad (9)$$

Equations (7) - (9) define the rating of the input rectifier and the DC link L-C filter.

3.1. CIRCUIT No. 1: CLASSIC INVERTER

This single rail circuit is presented in Fig. 1-a. It requires 2N active switches, where N is the number of motor phases. Although this is one of the oldest SRM inverter circuits [1], with a large number of switches, it is included in the analysis since it also has several advantages in low speed, high power drives.

The inverter operation is rather obvious and is reviewed briefly here for the sake of completeness. Since each phase is controlled independently from the others, one can consider just phase #1. The circuit has three possible states:

STATE 1: Magnetization
Both Q1 and Q2 are on, impressing the DC link voltage across the winding.

STATE 2: Free-wheeling
One phase switch is on while the other is off. The winding current free-wheels through the closed switch and the corresponding diode, but the rate of demagnetization is very low.

STATE 3: Forced demagnetization
Both Q1 and Q2 are off. The winding current flows through D1 and D2, against the DC link voltage, charging the capacitor C.

During low speed operation, only low-side switches, Q2-Q6 need to operate in PWM mode, with the inverter alternating between states #1, and #2. Note that state 2, with almost a constant current, leads to a low curent ripple, thus permitting low PWM frequency. The magnetizing and demagnetizing voltage Vdc has to be always larger than the motor CEMF.

The inverter design follows. Since the input rectifier and the L-C filter have been already defined at the beginning of this section, only switches Q1-QN and the diodes need be determined.

The peak voltage rating, transistors Q and diodes D, Fig. 1a, is:

$$VpQ = VpD = V\sqrt{2}(1 + DV) \qquad (10)$$

The transistor peak current, IpQ is defined by the motor starting requirement. Note that the current overlap does not affect switch rating since each phase operates independently.

The average energy returned to the inverter during each stroke is:

$$Wr = A/B \qquad (11a)$$

$$A = X * P; \qquad B = N * Nr * wn/(2\pi) \qquad (11b)$$

where A is the average power returned to the inverter by all phases while B is the total stroke frequency.

Thus, the device rating is:

Voltage rating, all devices:	$V\sqrt{2}(1 + DV)$
Current rating, all devices:	Ipw
Total active devices kVA:	$2N * Ipw * V\sqrt{2}(1 + DV)$

The current RMS and peak values can be determined only if the motor design and control angles are known. In order to satisfy braking operation, the diode current rating should be equal to that of the transistors.

The main advantages of the "classic" converter, Fig. 1a are the independent control of each of the motor phases and the relatively low voltage rating of the inverter components. The main disadvantages are the total number of switches, the DC link filter and a relatively low demagnetizing voltage at high speeds.

3.2. INVERTER CIRCUIT No. 2

This single rail inverter circuit has been reported by T. Miller [7] and is shown in Fig. 1b. This circuit is derived from the "classic" inverter by substituting the switches Q1, Q3 and Q5 by QA and the diodes D2, D4 and D6 by DA. In this way, the number of switches as well as the number of motor leads is reduced to N+1. The circuit has three operating states, which are analogous to those in the "classic" inverter. Considering phase #1:

STATE 1: Magnetization
Switches QA and Q1 are closed and the DC-link voltage is connected across the winding.

STATE 2: Free-wheeling
QA is closed, Q1 is open and the current free-wheels through QA and D1. The flux remains practically constant.

STATE 3: Forced demagnetization
Both QA and Q1 are off. D1 and DA conduct and the magnetic energy is transfered to the capacitor C. The demagnetization proceeds quickly, against the DC link voltage.

The main limitation of this inverter is that with QA on, a forced demagnetization of any of the phases is not possible. Consider first operation at low speed, with a PWM control of the winding voltage. In order to provide at least some demagnetizing voltage to another phase, Q1 is on while QA is PWM-controlled. If the duty-cycle is sufficiently low, that is, if the effective voltage, VY, applied to the winding of phase 1 is sufficiently small, another phase can still be demagnetized with the voltage Vdc-VY. As the voltage required by the winding increases with the motor speed, the voltage at Y-point is increased and the demagnetization voltage, Vdc-VY is decreased. Thus, when using this inverter circuit, one needs to calculate the limiting speed, bellow which there is a sufficient demagnetization voltage, even with a tail overlap. Experience indicates that with high speed SRMs, having a relatively low inductance per pole, this value approximately corresponds to VY = 0.5Vdc.

The device ratings are essentially the same as for the "classic" inverter, except for the QA and DA currents, which are, under the worst-case condition of a dwell overlap during motor starting, approximately twice the phase winding current.

Voltage ratings, all devices: $V\sqrt{2}(1 + DV)$
Current rating D1-D1 and Q1-Q1: Ipw
Current rating QA and DA: 2Ipw
Total kVA, active devices: $(N + 2) * Ipw * V\sqrt{2}(1 + DV)$

As it will be seen, this topology offers the lowest inverter kVA and is clearly advantageous providing that the current overlap does not pose a problem.

3.3. INVERTER No. 3: BUCK-BOOST CIRCUIT

This dual rail circuit with N+1 active switches is presented in Fig. 1c. To the best of our knowledge, this circuit has not been published before. The circuit offers an added flexibility in motor control by separating the magnetizing (Vc1) from the demagnetizing (Vc2) voltage. Considering the phase 1 only, the inverter operation can be divided into four states:

STATE 1: Magnetization
Q1 is closed, impressing the Vc2 voltage across the winding.

STATE 2: Forced demagnetization
Q1 is turned-off. D1 conducts, transferring the winding magnetic energy to C1. The voltage across Q1 is Vc1 + Vc2.

STATE 3: Discharging of C1
QA is on, discharging C1 while building the current in L2. Note that the AC line contributes to the L2 current.

STATE 4: Charging of C2
QA is turned off. DA conducts, transfering the energy stored in L2 to C2. The voltage across QA is Vc1 + Vc2.

The following comments can be made with respect to the operation of the buck-boost inverter:

- Each phase can be controlled independently, so that current overlap is not a problem. In fact, the states are completely non-interacting and state 1 can exist concurrently with states 3 and 4. The same is true for state 2, so that the chopper boost action can start during the demagnetization period in order to limit the voltage overshoot on C1.

- The C2 capacitor voltage is regulated continuously to satisfy the magnetizing requirements at each motor speed. In this way, PWM control of Q1-Q3 is not necessary, simplifying the driver design.

- If desired, it is possible to boost the C2 voltage significantly above the AC rectified voltage Vc1, thereby increasing the motor maximum speed for a given AC line voltage. (However, for a given inverter power, QA rating is minimum when Vc1 = Vc2. Also, the current tails would be longer than the dwell period).

- It is possible to reduce the AC line harmonics by eliminating L1, reducing C1 and using the boost chopper to waveshape the AC line currents. In this case however, a degree of freedom is lost and a compromise needs to be made between regulating the C2 voltage and waveshaping the AC input currents.

The ratings of the inverter components are now determined, starting with a chopper. Consider a motor at a start-up, with CEMF = 0. Assume that the winding current is constant and equal to its peak value Ipw. Assume further that there is a dwell overlap between the two phase currents so that the average current supplied by C2 is 2Ipw. The same current has to be supplied by the diode DA:

$$IdcDA = Idc\ C2 = 2 * Ipw \qquad (12a)$$

If the QA modulation index is m, then during the interval m the DA current is zero, while during 1-m interval it is equal to the L2 current:

$$IdcDA = (1 - m) * IdcL2 \qquad (12b)$$

Also, the peak QA current is:

$$IpQA = IdcL2\ (1 + R) \qquad (12c)$$

where R accounts for the current ripple ΔI in L2:

$$\Delta I = R * IdcL2$$

From (12a), (12b) and (12c) the current rating of the chopper switch QA is:

$$IpQA = 2 * (1 + R) * Ipw/(1 - m) \quad (13)$$

The last expression can be simplified. Consider:

$$m * Vc1 = (1 - m) * Vc2$$

Assuming that at a start up the Vc2 voltage is regulated to be 3% of the Vc2 voltage, one obtains m = 0.029. Furthermore, assuming very conservatively that the current ripple in L2 is 5%, so that R = 0.05, the final rating for QA becomes:

$$IpQA = 2 * 1.08 * Ipw = 2.16 * Ipw \quad (13b)$$

The RSM current in the chopper inductance L2 is:

$$IrmsL2 = (IdcL2)\sqrt{1 + R^2/3} \quad (14)$$

The chopper inductance is:

$$L2 = Vdc/(4 * fc * R * Idc) \quad (15a)$$

where fc is the chopper's PWM frequency.

The capacitor C1 should not be smaller than:

$$C1(min) = Wr/(DV * Vdc^2) \quad (15b)$$

where the energy returned to the inverter during demagnetization, Wr, is given by (11).

However, the capacitor value will be most likely determined based on the RMS current rating:

$$IrmsC1 = \sqrt{Ia^2 + Ib^2 + Ic^2} \quad (16a)$$

where Ia is the AC current component flowing through L1:

$$Ia^2 = (IrmsL1)^2 - (Idc)^2 \quad (16b)$$

while Ib is the AC component flowing through QA and L2:

$$Ib^2 = (IrmsL2)^2/2 - (IdcL2/2)^2 = (P/Vdc)^2 (1 + 2 * R^2/3)/4 \quad (16c)$$

The AC component of all tail currents, denoted by Ic and flowing through C1 during the demagnetization period can be calculated once the motor characteristics and the control parameters are known.

The capacitor C2 is also selected on the basis of the total AC current components:

$$IrmsC2 = \sqrt{Ib^2 + Id^2} \quad (17)$$

where Ib is the AC component of the diode DA current, equal to that of QA (because of 50% duty-cycle) and given by (16c), while Id is the AC component of the winding currents. To calculate Id, one has to know the waveform of the phase currents. One should check that the C2 value, calculated from (17) is not smaller than:

$$C2(min) = IdcL2/(4 * fc * Vdc * DV) \quad (18)$$

where DV is the allowed percentage voltage overshoot on C2. This overshoot is obviously determined by the dynamics of the voltage regulator, controlling QA. With a high chopping frequency fc and a fast chopper regulator, both L2 and C2 can be relatively small.

Assuming for the moment that voltage overshoots on C1 and C2 are equal, that is DVc1 = DVc2 = DV, the component ratings of the buck-boost converter are:

- Voltage rating for all devices: $2V\sqrt{2}(1 + DV)$
- Current rating for Q1-QN and D1-DN: Ipw
- Current rating for QA and DA: 2.16 Ipw
- Total kVA, active devices: $2 * (N + 2.16) * Ipw * V\sqrt{2}(1 + DV)$.

The main advantages of the buck-boost inverter are the flexibility in motor control, the ability to tailor the C2 voltage to the motor needs and thus avoid a PWM control of the phase switches, the non-interactive winding control, permitting current overlap, and the possibility of waveshaping of the input currents. The main disadvantage is the required double voltage rating on all devices, the need to process the entire motor input power through the chopper, and the large number of passive components.

3.5. INVERTER CIRCUIT No. 4: C-DUMP

This circuit, shown in Fig. 1d has been described by Ehsani et al [3]. It is a dual rail circuit, transposed with respect to the buck-boost inverter: the motor phases are supplied from the rectified voltage stored on C2, while the magnetic energy, stored in C1, is transfered to C2 through the chopper consisting of QA, L1 and DA. If one were to connect the input rectifier and the L1 inductance of the buck-boost circuit across its C2 capacitor, one would obtain a modified C-dump circuit, where the capacitor C1, Fig. 1d is re-connected between QA and point H. Such modification would be desirable, since the voltage available for demagnetization would be Vc1 instead of Vc1-Vc2 as in Fig. 7d. (Or, with the same demagnetizing voltage, the voltage rating of C1 would be approximately halved.) However, this paper will consider the original circuit, as reported in [3]. The inverter has four possible operating states, functionally identical to those in the buck-boost inverter. Considering phase 1:

STATE 1: Magnetization
Q1 is on and C2 is connected across the winding, supplying the magnetizing energy.

STATE 2: Forced demagnetization
Q1 is turned off and the demagnetizing current circulates through D1, C1 and C2. The rate of demagnetization is determined by the voltage difference Vc1-Vc2. The voltage across Q1 is Vc1.

STATE 3: Discharging of C1
QA is on and the current loop is closed through L1, C2 and C1. The C2 voltage increases as the current builds up through L1.

STATE 4: Completion, charging of C2
QA is off, the current circulates through L1, C2 and DA, transferring energy stored in L1 to C2. The voltage across QA is Vc1.

The C-dump is very similar to the buck-boost inverter and the same comments, given in the last section apply here. The only

differences between these two circuits are:

- Since the phases are supplied from the uncontrolled rectified voltage Vc2, each phase switch, Q1-QN needs to perform PWM control at low speed. As a result, a large portion of the energy is transfered to C1 and then again, through the chopper action, back to C2.

- By turning on simultaneoulsy Q1 and QA (operating concurrently in states 1 and 2) it is theoretically possible to increase the motor supply voltage and thereby increase the maximum motor speed. Such a mode of operation is called a synchronous chopper control in [3]. In practice, however:

  - Insertion of L1 inductance into the motor magnetizing loop is contrary to a desire for a fast magnetization at high speed
  - C1 is discharged during dwell period and becomes ill-prepared for the demagnetization requirements of a short current tail.

For these reasons, the maximum winding magnetizing voltage is practically fixed by the AC lines.

- For the same reason as above, wave shaping of the AC input currents and thus AC line harmonic control is not possible.

- Although the C-dump chopper has to process only the demagnetizing power XP instead of the full inverter power P in case of the buck-boost inverter, there is very little difference in their ratings, since both choppers have to be dimensioned for the starting currents, which are approximately the same for the two circuits.

The C-dump components can be selected using the same equations as for the buck-boost circuit, with these exceptions:

$$IdcL1 = X * P/Vdc \qquad (19)$$

where P is the rated converter power P = Pn/(1 - X), and XP the demagnetizing power transferred from C1 to C2. Also the expression for the minimum value of C2 has to be modified. With the C-dump circuit, the total energy stored in C1 is:

$$WrC1 = W1 + W2$$

where W1 comes from the winding magnetic energy, eq. 11a, and W2 comes from the capacitor C2. If Vc1 = Vc2, W1 = W2, so that the energy stored on C1 is 2Wr. This energy needs to be transferred through the chopper to C2 which then becomes:

$$C2(min) = 2Wr/(DV * Vdc^2) \qquad (20)$$

or twice the value given by eq. (15b) for the corresponding capacitor in the buck-boost inverter.
To size QA, consider the motor just starting. Assume that Q1-QN are PWM-controlled with 50% duty-cycle, and that QA is also operating with 50% duty-cycle to give Vc1 = Vc2. Furthermore, assume that each phase draws the peak current Ipw and that there is a dwell overlap between the currents in two phases. Under these conditions, the average current charging C1 is 0.5 Ipw + 0.5 Ipw while the average current discharging C1 is 0.5 IdcL2. Obviously the charging and the discharging currents must be equal. Also, the peak QA current is:

$$IpQA = IdcL2\ (1 + R) = 2 * Ipw\ (1 + R) \qquad (22)$$

Assuming the ripple in L2 to be 5% (R = 0.05), the component ratings for the C-dump inverter become:

Voltage rating, all devices: $2 * V\sqrt{2}(1 + DV)$
Current rating, Q1-QN and D1-DN: Ipw
Current rating, QA and DA: $2.1 * Ipw$
Total kVA, active devices: $2 * (N + 2.1) * Ipw * V\sqrt{2}(1 + DV)$

3.5. INVERTER CIRCUIT No. 5

This circuit, presented in Fig. 1e. is the last dual rail topology considered here. Since this is a new circuit [8], its operation is discussed in some detail.

The main circuit characteristic is the elimination of a DC link inductance and a capacitor, and the direct transfer of the capacitor energy to the motor windings. It is believed that this is the minimum component topology. Although this circuit has similarity with C-dump inverter (and thus also with a buck-boost configuration) its modes of operation are fundamentally dif-rent. Considering phase 1, one can identify four operating states:

STATE 1: Magnetization from the AC line.
Q1 is closed and the phase winding is connected to the unfiltered rectified voltage Vr.

STATE 2: Magnetization from the capacitor.
Both Q1 and QA are closed. With the capacitor voltage Vc being larger than the rectified voltage Vr, the input rectifier is reverse biased and the energy flows from the capacitor to the winding. The supplied power is P2=(Vc)(Iw). If Vc<Vr QA is reverse biased and the operation reverts to state 1.

STATE 3: Demagnetization through free-wheeling.
QA and D1 conduct, short-circuiting the winding. The magnetic energy is discharged by a free-wheeling current, but the demagnetization is very slow, depending entirely on the circuit resistance. Q1 has to withstand Vc.

STATE 4: Demagnetization by charging the capacitor.
Both Q1 and QA are turned off. The winding is demagnetized through D1, capacitor C and the input rectifier, which provides the free-wheeling path. The capacitor is charged by energy transfer from the winding and by the AC line. The energy Wr returned from the winding is:

$$Wr = (Vc - Vr) \int iw(t)dt$$

The total energy received by the capacitor is:

$$Wc = Vc \int iw(t)dt = [Vc/(Vc-Vr)]Wr \qquad (24)$$

Due to the four possible states, the inverter control is complex, while at the same time giving additional freedom in controlling the motor. The following comments apply:

- The capacitor voltage has to be kept within a relatively narrow band. Its minimum value, defined by the demagnetizing requirements, should be as high as possible. Its maximum value, on the other hand, determines the capacitor and thus all transistor ratings and should be as low as possible.

- For the capacitor to maintain an average constant voltage, the energy taken (state 2) must equal the energy given(state 4).

- During the low speed operation, the phase switches have to be PWM controlled thus alternating between state 1 and state 4. (The circuit operates then as a step-up chopper). A rise in the capacitor voltage due to state 4 can be controlled by transferring the operation from state 1 to state 2.

- State 3 is used for demagnetization only at very low speeds, when the time is not critical. Providing that the capacitor is adequately charged, state 3 can be used during a PWM operation to permit reduced PWM frequency for the same ripple.

- During forced demagnetization, state 4, the switch QA has to be off until the current in that phase is reduced to zero. Table 1 summarizes the various states which can concurrently exist between the two adjacent phases.

		Phase A			
P	State	1	2	3	4
h	1	yes	no	no	yes
a B	2	no	yes	yes	no
s	3	no	yes	yes	no
e	4	yes	no	no	yes

Table 1: *Possible concurrent states.*

- Theoretically, one could extend the motor speed range by operating in state 2, connecting the capacitor voltage across the winding. In practice, state 2 is used only to control the capacitor voltage, with the increase in the winding magnetizing voltage only secondary. The reason is that the capacitor does not have a sufficient charge to sustain a phase current during a dwell period. If one tries to replenish this charge by a winding PWM control (boost-up chopper) at high speeds, one would reduce the total volt-seconds applied to the winding during the dwell period, because of the chopper losses. However, the magnetic energy, transfered to the capacitor at the end of each stroke, will somewhat increase the available magnetizing voltage and thus the maximum motor speed.

- The inrush current problem is eliminated since the capacitor is always pre-charged through one of the phases. This also means that the motor will rotate through a portion of a turn at each power-up.

- Since all active switches have to be capable of PWM operation, all gate drivers need to be adequately designed and all diodes should be of the fast type.

- With the DC link capacitor eliminated, the AC line is not buffered from the motor current pulses and the line harmonics may be a problem.

To determine the rating of the inverter components, consider first that the minimum capacitor voltage, necessary for a demagnetization, has to be:

$$Vc(min) > CEMF + V\sqrt{2} \qquad (25)$$

where CEMF is the motor counter EMF and V is the line to line voltage, AC input. Thus, one needs to determine the motor CEMF. Consider first the dwell period Td:

$$Td = Tc + Tl$$

Tc - total time during dwell when the capacitor voltage is impressed across the phase winding.
Tl - total time during which the rectifier line voltage, Vr, is impressed across the winding. Then:

$$CEMF = (Tc * Vc + Tl * Vr)/Td = ml * Vr + (1 - ml)\, Vc \qquad (26)$$

where ml is the rectified voltage duty-cycle during the dwell period. The total energy given to the winding during the dwell is:

$$Wt = Td * Iw * CEMF = Td\,(ml * Vr + (1 - ml)\, Vc) * Iw =$$

$$= Wlm + Wcm \qquad (27)$$

where Wlm and Wcm are the energies transferred to the motor from the AC line and the capacitor, respectively.

During the demagnetization, the motor returns to the capacitor a portion X of the total energy Wt:

$$Wr = X * Wt = X * Td * Iw * CEMF \qquad (28)$$

The total energy transfered to the capacitor is:

$$Wc = Wr + Wlc \qquad (29)$$

where Wlc is the energy supplied by the AC line to the capacitor. Also from (24):

$$Wc = Wr * Vc/(Vc - Vr) = X * Td * Iw * CEMF * Vc/(Vc - Vr) \qquad (30)$$

$$Wlc = X * Td * Iw * CEMF * Vr/(Vc - Vr) \qquad (31)$$

The capacitor energy is constant so that the energies supplied and received must be equal:

$$Wc = Wcm \qquad (32)$$

Also, the energy supplied by the line and converted into mechanical work:

$$Wl = Wlm + Wlc = Wn = (1 - X)\, Wt \qquad (33)$$

From (32) and (33) it follows:

$$X * Vc/(Vc - Vr) = (1 - ml) * Vc/CEMF \qquad (34)$$

$$X * Vr/(Vc - Vr) + ml * Vr/CEMF = (1 - X) \qquad (35)$$

From which is obtained the maximum motor voltage:

$$CEMF = Vr/(1 - X) \qquad (36)$$

The last expression is simplified by replacing the rectified voltage Vr by Vdc. The capacitor voltage rating, from (25) is:

$$Vc(min) = (V\sqrt{2} + Vdc/(1 - X))\,(1 + DV) \qquad (37)$$

Eq. (36) and (37) indicate that an increase in the returned

energy X allows higher motor speed for the same AC line voltage while, at the same time, increasing the capacitor voltage rating. Using a typical value, X = 0.25, the voltage rating becomes:

$$Vc(min) = 2.27\ V\sqrt{2}\ (1 + DV) \quad (38)$$

The capacitor minimum value is:

$$Cmin = Wr/(2.27V * DV\sqrt{2}) \quad (39)$$

where Wr is defined by (11a). The capacitor size is normally determined by its RMS current rating. First:

$$CEMF = mc * Vc + (1 - mc) * Vdc \quad (40)$$

where mc is the modulation index of QA, and can be calculated for a worst case condition from (36) and (40). The capacitor RMS current is then:

$$Irms\ C = \sqrt{Ia^2 + mc * (Iwrms^2 - Iwdc^2)} \quad (41)$$

where Ia is the AC component of current tails, during demagnetization.

To determine the current rating of QA, consider the motor just starting. Assume that Q1-QN are PWM controlled with a 50% duty-cycle and that QA is also operating with a 50% duty-cycle (to allow for demagnetization). Assume that there is a dwell overlap and that each operating phase draws the full peak current Ipw. The tail current from the two phases charging the capacitor are 0.5Ipw and 0.5Ipw. The capacitor is discharged with an equal current of Ipw which passes through QA. Since QA operates with a 50% duty-cycle, its peak current is 2Ipw. As a result, the inverter device ratings are:

Voltage rating, all devices: $2.27V\sqrt{2}\ (1 + DV)$
Current rating, Q1-QN and D1-DN: Ipw
Current rating QA and DA: 2Ipw
kVA rating, active devices: $2.27\ (N + 2) * Ipw * V\sqrt{2}\ (1 + DV)$

3.6. SUMMARY

The general discussion presented in this section indicates that all dual rail inverters suffer from a requirement for a minimum voltage rating of approximately twice the motor supply voltage. For that reason, single rail inverters, Figures 1a. and 1b. will be most likely the choice for 380V and 460V industrial SRM drives. Of these two, the N + 1 topology, Fig. 1b. is clearly prefered if the restriction posed by a current overlap can be resolved. (There is no restriction for the overlaps occuring below the speed at which the demagnetizing voltage is more than twice the magnetizing voltage).

Finally, one should note the circuit comparison based on the required inverter kVA is only one of the criteria to be used and that one, after narrowing the choice, should do a more detailed analysis to justify the final selection.

4. NUMERICAL EXAMPLE - HIGH SPEED DRIVE

In order to illustrate the design procedure given in the last section, a design for a high speed drive is now presented. The design is carried out for each circuit given in Fig. 1. The AC line supply voltage is 380V, 50Hz. The drive uses a high speed 6/2 motor, schematically shown in Fig. 2. and suitable for spindle applications. The motor has the following characteristics:

- Four low speed poles, with 120 turns per pole
- Two high speed poles, with 70 turns
- Base speed 3100RPM
- Maximum speed 20000RPM
- Rated torque 30.8Nm
- Rated RMS current 47.5A
- Rated peak current 111A
- Rated efficiency 86%.

In order to achieve the desired speed range, 0-20000RPM, Fig. 8., the motor control strategy requires a special attention. As discussed in section 2, symmetrical SRMs are ill-suited for constant power operation over extended speed range, since, with a fixed dwell angle and a constant supply voltage, the motor

Table 2: Operating points and configurations for the 6/2 motor.

POINT / QUANTITY	1	2	3	4	5	6	7	8	9	10
SPEED, RPM	0	690	2000	3100	5000	8000	8000	10500	10500	20000
CONFIGURATION	6/2	4/2	4/2	4/2	4/2	4/2	2/2 SLOW	2/2 SLOW	2/2 FAST	2/2 FAST
MAGNET/DEMAGN. VOLTAGE, VOLTS	15/515	102.4/515	241/515	391/515	515/515	515/515	441/515	515/515	398/515	515/515
DWELL/CONDUCT. ANGLES	90/95	50/57	46/69	38/64	36/72	54/108	67/112	72/144	59/107	69/137
PHASE PEAK CURRENT, A	111	101	101.5	111	92.9	85.76	104	110	108.5	104
PHASE RMS CURRENT, A	78	45.7	44.5	47.5	38	33.42	45.7	54	50	46.9
TOTAL TORQUE, Nm	11*	34.5	34.25	32.75	20.4	12.75	12	9.1	9.1	4.77
TOTAL POWER, W	0	2492	7173	2492	10681	10681	10053	10005	10005	10000
RETURNED ENERGY RATIO, X		0.21	0.24	0.23	0.25	0.22	0.19	0.23	0.2	0.19

* WORST - CASE ROTOR STARTING POSITION

power becomes inversely proportional to the speed.

In order to reconcile the high and low speed requirements, one needs to modify motor configuration as the speed is increased. Fortunately, SRMs are amenable to such approach and the 6/2 geometry offers several alternatives. In this case, a high speed winding, placed on the third phase, permits to practically double the motor speed from 11500RPM to 20000RPM. Table 2 gives information about the key motor operating points in the intended speed range. This points are then used in the design of the drive inverters. The following comments apply:

- With 6/2 motor, the torque at a standstill is typically produced by only one pole-pair. Furthermore this torque greatly depends on the rotor position. For the worst-case, the nominal torque at standstill requires 208A in the two low speed windings and 217A in the high speed winding. An inverter rated for these starting currents would be obviously oversized and uneconomical. Given the high speed application of the 6/2 motor, the decision became to restrict the starting currents to nominal peak value and to design all inverters accordingly. The worst-case starting torque is therefore reduced to 11Nm or 37% of the nominal torque. Note that, statistically, the starting torque will be higher, but 11Nm is the absolute minimum value.

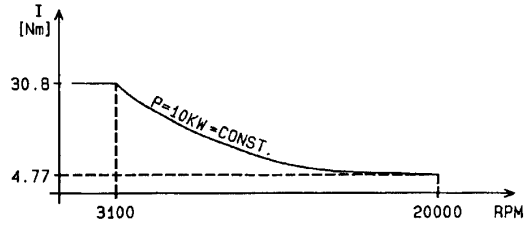

Fig. 8.: speed-torque boundary of the 10kW 6/2 motor

- In considering motor control, a full demagnetization voltage of 515V is assumed. Any reduction of this voltage will change the ratio between dwell and conduction angles, resulting in decreased torques.
- At low speeds, the high speed winding is inefficient and is switched off as soon as the motor has started.
- From standstill to 5000RPM, the magnetizing voltage is gradually increase, until all available voltage is used. However, at 5000RPM, the dwell angle is very short (the optimum dwell angle is approximately 67°) and the currents are relatively small. With the available magnetizing voltage fully utilized, the dwell angle is increased to maintain constant power from 5000 to 8000RPM.
- At 8000RPM the operation is switched to 2/2 configuration with a low speed winding, primarily for the reasons of the drive effiency.
- At 10500RPM a switch to the high speed winding results in a lower inductance, permitting a decrease in current advance and a reduction of the current peaks. At the same time, the applied voltage can be reduced, leaving room for a further speed increase.
- At 20000RPM the motor is using all available voltage and is operating close to its maximum dwell angles. A further increase in speeds would result in a reduction of the output power.
- The current overlap exists at every point below 8000RPM except the point #2, for control giving the same dwell and conduction angles to each phase.
- In the inverter design, each component is rated to enable the drive operation at each point listed in Table 2. Alternately, the control is changed and the new operating points are defined (case of the circuit #2).

With the motor load defined, the inverter design is carried out using the procedure outlined in the last section. First, taking into account the motor efficiency and using X = 0.25, the line rectifier and the DC link filter are:

from eq. (6b)	P = 15.5 kW
from eq. (7)	Idc = 30 A
from eq. (8c)	IrmsC = 79 A
from eq. (9) and (11)	Cmin = 353 microF.

The numerical design is carried for each circuit of Fig. 1. A 5% current ripple (R) and a 20% voltage ripple (DV) are assumed throughout the design.

4.1. CIRCUIT No. 1: CLASSIC INVERTER

From eq. (10)	VpQ = VpD = 645 V
from eq. (11a)	Wr = 18.75 joules
from point #4, Table 2	IpQ = 111 A
the kVA, active devices	429.5 kVA

4.2. CIRCUIT No. 2

Since this circuit has restrictions with respect to current overlaps, the motor control shown in Table 2, has to be modified in the range of 2000-8000 RPM. First, bellow 2000RPM, the magnetizing voltage (VY, Fig. 1b.) is always less than half the demagnetizing voltage and the overlap does not pose a problem. From 2000-8000RPM one should control the motor in the following way:

- From 2000 to 5000RPM the magnetizing voltage is kept bellow half the demagnetizing voltage while the power increase is obtained by widening the dwell angle. The motor operates in the 4/2 configuration.

Table 3: *Points with modified control for Circuit #2.*

QUANTITY \ NEW POINT	PHASE	4a	5a	5b	6a
SPEED, RPM		3100	5000	5000	80000
MAGNET/DEMAGN. VOLTAGE, VOLTS	B	241/515	257/515	277/515	398/515
	C	SAME	SAME	515/515	515/515
DWELL/CONDUCT. ANGLES	B	55/80	67/100	67/107	67/118
	C	SAME	SAME	23/46	23/46
PEAK CURRENT, A	B	114	95	105	98
	C	SAME	SAME	110	101
RMS CURRENT, A	B	51	42.2	46	42.6
	C	SAME	SAME	41.2	39.58
RETURNED ENERGY RATIO, X	B	0.21	0.24	0.2	0.22
	C	0.21	0.24	0.24	0.23
TORQUE, Nm	B	15.5	9.87	11.85	9.5
	C	15.5	9.87	8.15	2.5
TOTAL POWER		10063	10335	10471	10053

- From 5000 to 8000RPM, the phase dwell angles are controlled unsymmetrically. To illustrate, assume that in Fig. 2, the phase A is the high speed (not used) phase and that the rotor is turning clockwise. Then the phase C is controlled with a wide and the phase B with a narrow dwell angle. As the speed approaches 8000RPM the contribution of phase B decreases until, at 8000RPM, the phase B is disconnected and the motor continues in the 2/2 configuration with the phase C. From then on, the motor is controlled as in Table 2.

Table 3 defines the modified operating points for the inverter circuit No. 2.

The ratings of all components for circuit No. 2 are the same as for the circuit No. #1 except for the chopping switch QA and the diode DA which must be rated for 2Ipw = 222 A to provide the overlapping starting currents.

The total kVA of the active devices is 357.9 kVA.

4.3. CIRCUIT No. 3: BUCK-BOOST INVERTER

This circuit has no overlap restriction so that control defined in Table 2 is used.

From eq. (12a)	IdcDA = 222 A
from eq. (12b)	IdcL2 = 233.6 A
from eq. (13b)	IpQA = 239.7 A
from eq. (14)	IrmsL2 = 234 A
from eq. (15a)	L2 = 2.8 mh
C1(min) is the same as for Circuit #1	
from eq. (18)	C2(min) = 141 microF
the total kVA for active devices is:	738.7 kVA

4.4. CIRCUIT No. 4: C-DUMP INVERTER

The rating of all phase switches, Q1-Q3 and the feedback diodes D1-D3 is the same as in the buck-boost inverter. The rating of L2 is the same as that for L1 in the "classic" inverter. The minimum value for the DC link capacitor C2 is:

from eq. (20)	C2(min) = 706 microF
from eq. (22)	IpQA = 233.1 A
the kVA rating, all active devices is:	730 kVA

4.5. CIRCUIT No. 5

The current rating of the phase switches Q1-Q3 and the diodes D1-D3 is the same as for the other inverters (111 A). The current rating for QA and DA is 222 A. The voltage rating for all devices, from eq. (38) is 1462 Volts. The total kVA, for the active devices is 812.8 kVA.

4.5. DISCUSSION

From the numerical results one draws the same conclusion as in section 3: if the current overlap restriction can be resolved, the circuit No. 2, Fig. 1b., gives the most economical topology. The dual rail circuits are penalized by the high required voltage rating and are not justified in industrial drives supplied from 380 or 460 Volt AC line.

5. NUMERICAL EXAMPLE: HIGH TORQUE DRIVE

The design procedure given in section 3 is used here to evaluate numerically the suitability of the five, four-phase inverter circuits, Fig. 1., for a low speed, high torque, drive. The drive uses a 8/6 motor, schmatically presented in Fig. 3. having the following characteristics:

Number of phases	4
Rated voltage	510 V
Rated peak current	63.35 A
Rated RMS current	26.12 A
Rated speed	3000 RPM
Rated torque	31.83 NM
Rated power	10 kW

The motor is controlled with a dwell angle of 13°and a conduction angle of 26°, which leads to a current overlap. In order to eliminate the overlap, the dwell angle is reduced to 8° in the case of circuit #2, leading to an inefficient design, which is included here only for comparison.

The numerical results for the key inverter components are summarized below. A 5% current and 20% voltage ripple are assumed and each inverter circuit of Fig. 1. is modified to include four phases.

CIRCUIT #1: classic inverter

Voltage rating, all devices:	645 Volts
Current rating, all devices:	63.85 A
Total kVA, active devices:	329.5 kVA

CIRCUIT #2

Since the dwell angle has to be reduced to 8° to avoid the current overlap, the currents are increased so that the peak current for each phase becomes 137A. The device ratings are then:

Voltage rating, all devices:	645 V
Current rating, phase switches:	137 A
Current rating, chopper switch:	274 A
Total kVA, active devices:	530 kVA

CICRUIT #3: Buck-boost inverter

Voltage rating, all devices:	1290 V
Cuirrent rating, phase devices:	63.85 A
Current rating, chopper devices (QA and DA):	137.9 A
Total kVA, active devices:	507.3 kVA

CIRCUIT #4: C-dump inverter

Voltage rating, all devices:	1290 V
Current rating, phase devices:	63.85 A
Current rating, chopper devices (QA and DA):	134 A
Total kVA, active devices:	502.3 kVA

CIRCUIT #5:

Voltage rating, all devices:	1463 V
Current rating, phase devices:	63.85 A
Current rating, chopper devices (QA and DA):	127.7 A
Total kVA, active devices:	560.4 kVA

From these results, the classic inverter, circuit #1 is the clear choice. In fact none of the other circuits could be really used in this application: circuit #2 is not good since it leads to poor inverter and motor utilization with too narrow dwell angles. All other circuits with dual rail topology are not applicable because of the unacceptable voltage ratings.

it is interesting to compare the required inverter kVA for the 6/2 and 8/6 motors which leads to a tentative conclusion that low speed motors require less "peaky" currents and thus, for the same motor power, require less installed inverter kVA.

6. EXPERIMENTAL RESULTS

The experiments were performed with the inverter circuits, Fig. 1., No. 1 (classic), No. 2., No. 3., (buck-boost) and No. 5., on the high-torque experimental 8/6 motor. The dimensions of the stator and rotor poles are given in Fig. 9., while the motor parameter are:

Axial lenght	139mm
Rotor diameter	103mm
Airgap	0.3mm
Number of turns per pole	28
Resistenca per phase	70mohms
Aligned inductance, at 50mA	15.1mh
Non-aligned inductance at 50mA	2.24mh
Rated power	1600Watts

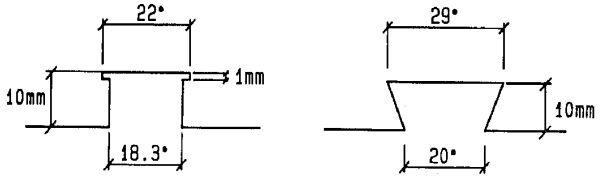

Fig. 9.: *details of the 8/6 motor*
a) stator pole
b) rotor pole

Since in case of circuit #5 the capacitor discharges through the motor winding, the PWM operation is present in the motor currents, Fig. 13.

- The capacitor discharge current, is highly distorting the input current in circuit #5, Fig. 13b.

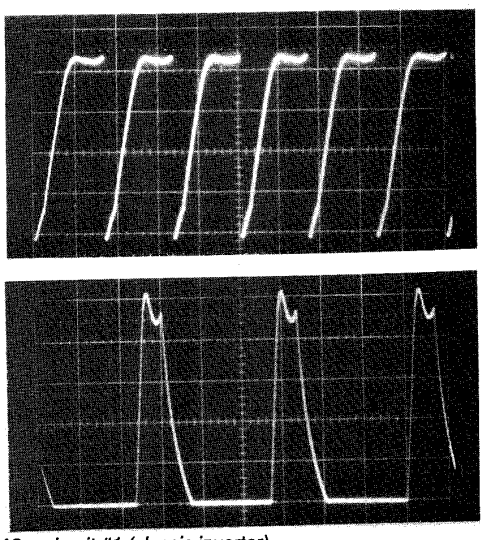

Fig. 10.: *circuit #1 (classic inverter)*
upper: DC link current, 10A/div. and 0.5ms/div.
lower: winding current, 5A/div. and 1ms/div.

VARIABLE / INVERTER	Vdc V	DWELL	Idc A	$I_{dc^{rms}}$ A	Iwp A	Iwrms A	IpD A	IpQA A	IrmsQA A	IpDA A	IcAP A
# 1 : CLASSIC	200	13	18.6	23.5	25.6	10.45	23.5	/	/	/	16.3
# 2 : CIRCUIT	305	8	7.81	22.6	36.1	11.3	24	36.1	19.8	35	22
# 3 : BUCK BOOST	195	13.3	-	-	26	10.5	22.57	40	21.6	40	16.73 / 17.1
# 5 : CIRCUIT	210	13.3	19.95	24.11	34.7	12.52	34.1	40.5	14.7	-	14.6

Table 4: *summary of experimental results.*

Note:The following subscripts are used in Table 4:
p - peak value
w - winding
QA - chopper switch/diode
D - phase diode

The motor was loaded appropriately and the starting (Os) and the dwell angles were adjusted to obtain the minimum current at each test point. The measured waveforms are shown in Figurres 10-13 while the results are grouped in Table 4.

The following comments apply:

- The circuit #2 is inappropriate for the 8/6 motor because of the current overlap restriction. To prevent the overlap, the dwell angle was restricted to 8°, while the current tail was 7°. The motor supply voltage had to be raised 50% to 360V in order for the motor to deliver the required 1.6kW power. The effect on the current pulse width is clearly seen in Fig. 11b.
- At this operating point, a 2kHz PWM control was used only on switches QA, Fig. 1c. and 1e. to control the capacitor voltage.

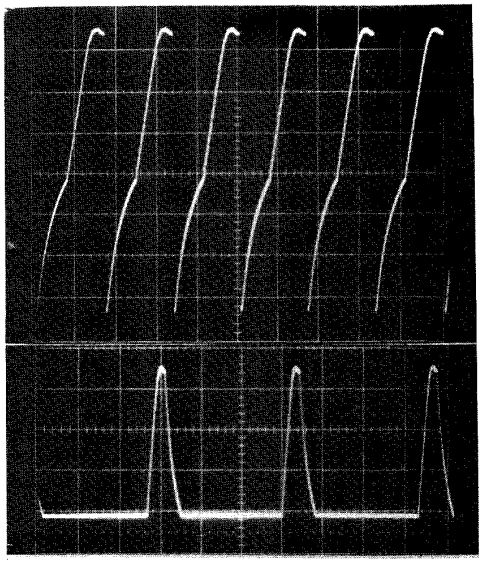

Fig. 11.: *circuit #2*
upper: DC link current, 10A/div. and 0.5ms/div.
lower: winding current, 10A/div. and 1ms/div.

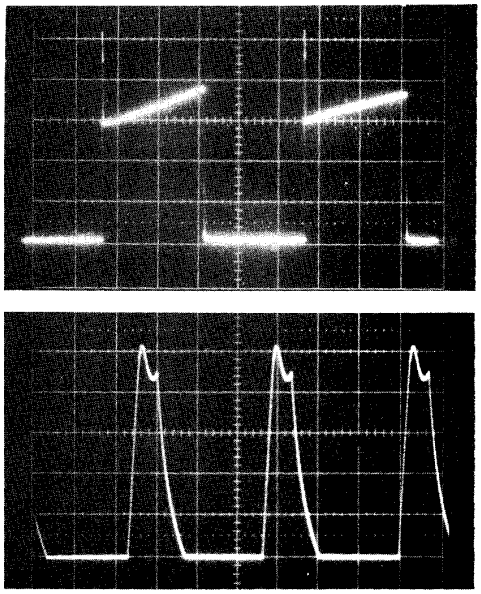

Fig. 12.: circuit #3 (buck-boost inverter)
upper: current, QA chopper, 10A/div. and 0.1ms/div.
lower: winding current, 5A/div. and 1ms/div.

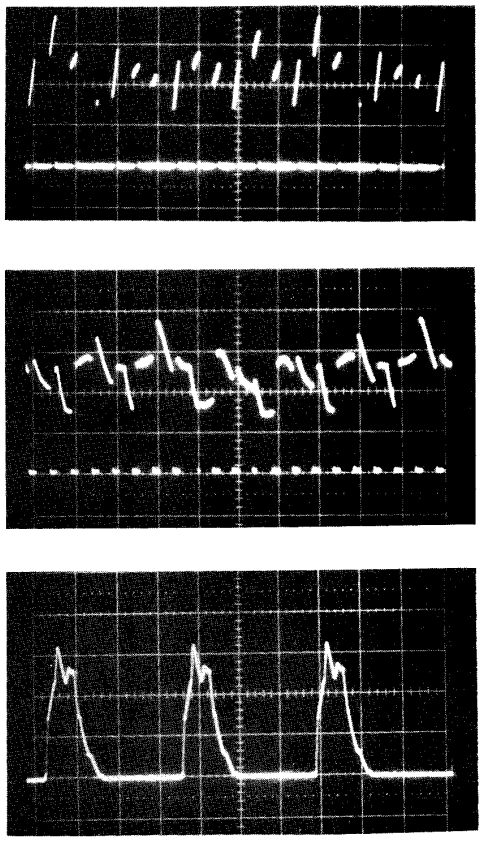

Fig. 13.: circuit #5
upper: current, QA chopper, 10A/div. and 0.5ms/div.
middle: rectifier output current, 10A/div. and 0.5ms/div.
lower: winding current, 10A/div. and 1ms/div.

7. CONCLUSION

The paper described two new inverter circuits, not published before, and gave a detailed design procedure for the five circuits which were considered. Out of these five, only two circuits were found suitable for industrial SRM drives, supplied from 380 or 460V AC lines. The remaining three circuits all use dual rail topology, and thus require that the inverter active devices have a rating at least twice the motor supply voltage. Consequently, the dual rail inverters may find applications in low power low voltage drives but are not suitable for industrial drives.

If the current overlap (interval over which the two phases conduct concurrently) can be restricted to speeds where the motor magnetizing voltage is below approximately one half the available demagnetizing voltage, the most advantageous circuit is the one reported by Miller [7]. However, since majority of SRMs operate with a current overlap over most of their speed range, the "classic" inverter, Fig. 1a., becomes the most attractive topology, in that case.

The need for a high PWM frequency is not as strong in SRM drives as in induction motor drives since the inverter output "sees" the total phase inductance and not only the leakage inductance as with the induction motors. That, combined with the free-wheeling inverter states identified in this study permits reduced PWM frequency for the same current ripple. As a result, it is expected that the resoonant type inverters will be less justified than with the induction drives.

Finally, a general comment is that regardless of the technical merrits of the SRM technology, an industrial use of SRMs in general purpose drives is most unlikely, given the need for an extremely close design coordination between the motor, the control and the inverter. That coordination has to be much closer than in the case of brushless drives and indicates that the SRM applications may be more successeful if directed towards unique, special purpose or OEM-type drives.

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